GLAST Large Area Telescope:

Calorimeter (CAL) Subsystem
WBS: 4.1.5

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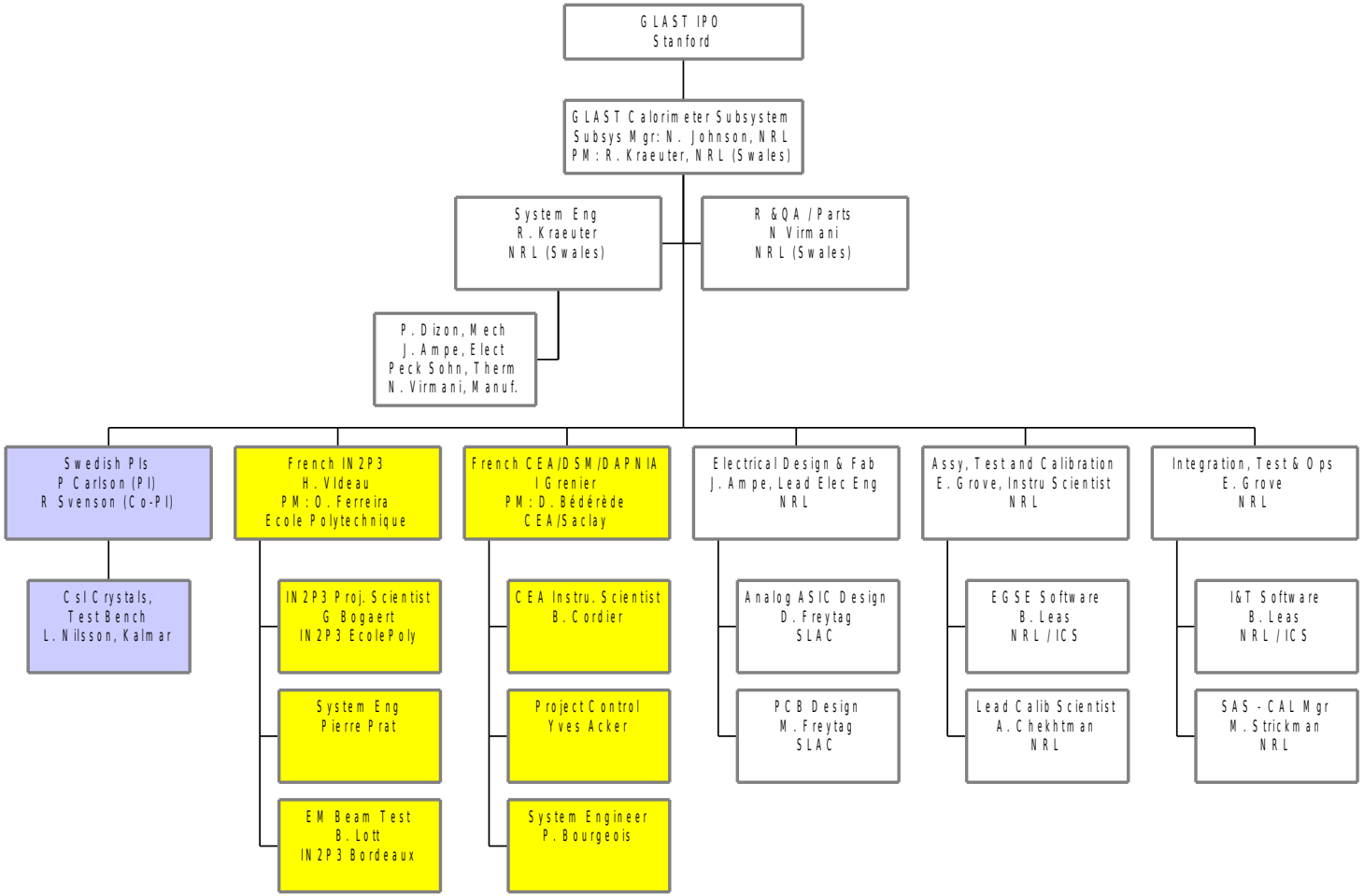
Outline

- Overview
- Requirements
- Design
- Verification Program
- Fabrication Process
- Cost and Schedule
- Risks and Summary

Overview

Section 8

Calorimeter – Institutional Organization

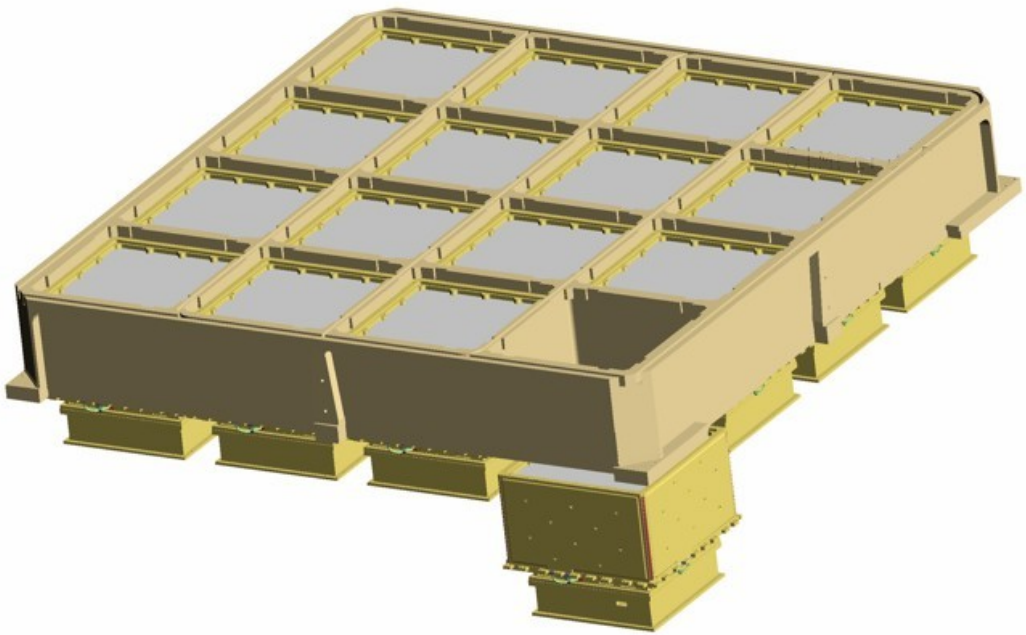


CAL Hardware Collaborators

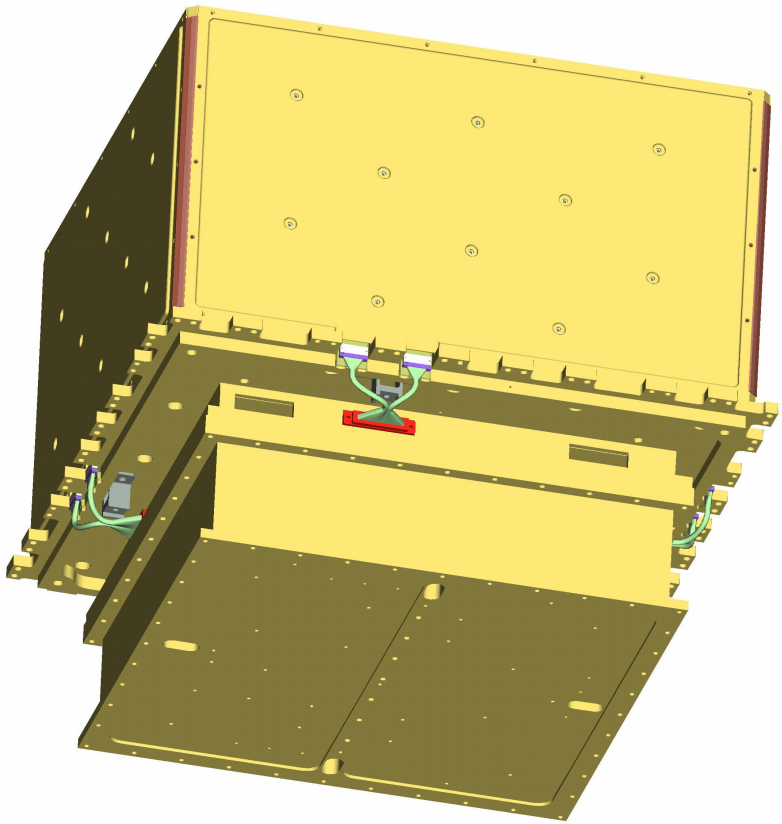
Organization	Responsibility
Naval Research Lab	CAL Subsystem Management & System Engineering Safety & Mission Assurance, Subsystem Design PIN photodiode spec and shared procurement CAL Electronics Design & Fab, Digital ASIC design, CAL Module Assy & Test, LAT I&T Support
SLAC	CAL Analog ASIC Design AFEE PCB layout
Sweden	CsI Crystal procurement and acceptance test
France / CEA	Crystal Detector Element design, fabrication and test Part of PIN photodiode procurement, PIN Diode assembly procurement, PIN-CsI bonding, CsI optical wrap.
France / IN2P3	Mechanical Structure design and fabrication Carbon composite cell structure. Al baseplate and closeout shells, elastomer bumpers and cords. Finite element and thermal analyses. Beam Test Planning and Support

Modular Design

4 x 4 Array of Calorimeter Modules



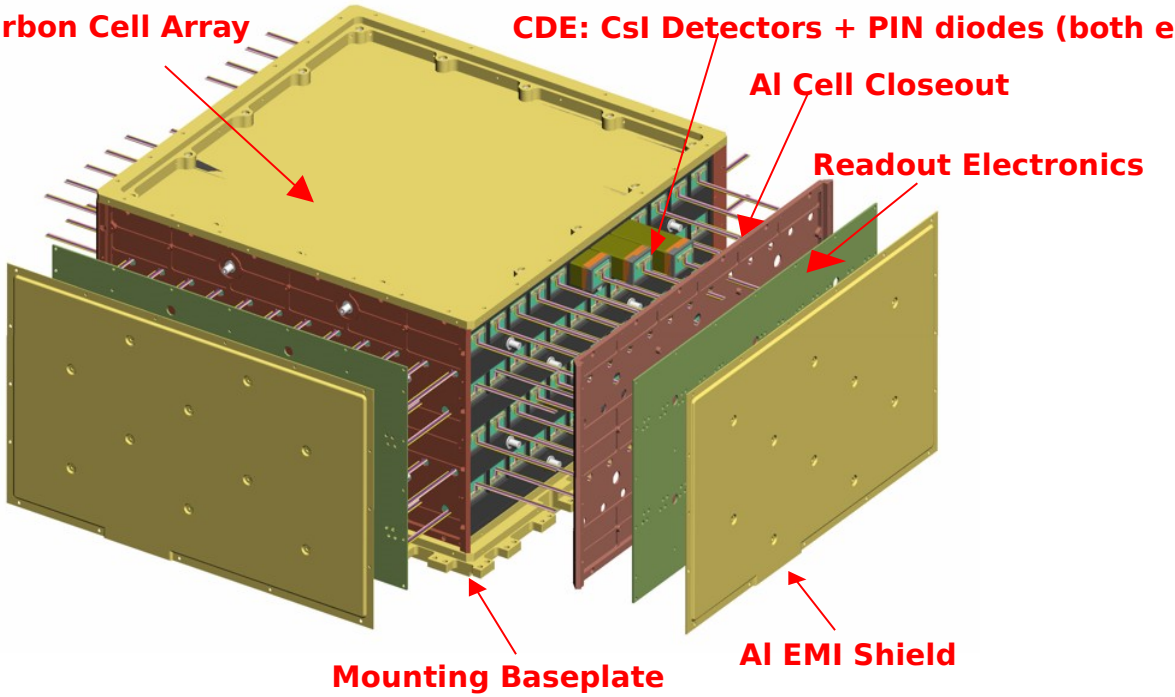
LAT GRID with16 CAL Modules



CAL Module with TEM and Power Supply mounted to base plate

CAL Module

- 8 layers of 12 CsI(Tl) crystals
  - Crystal dimensions
    - 27 x 20 x 326 mm
  - Hodoscopic stacking
    - alternating orthogonal layers
  - Dual PIN photodiode on each end of crystals
- Mechanical packaging
  - Carbon Composite cell structure
  - Al base plate and side cell closeouts



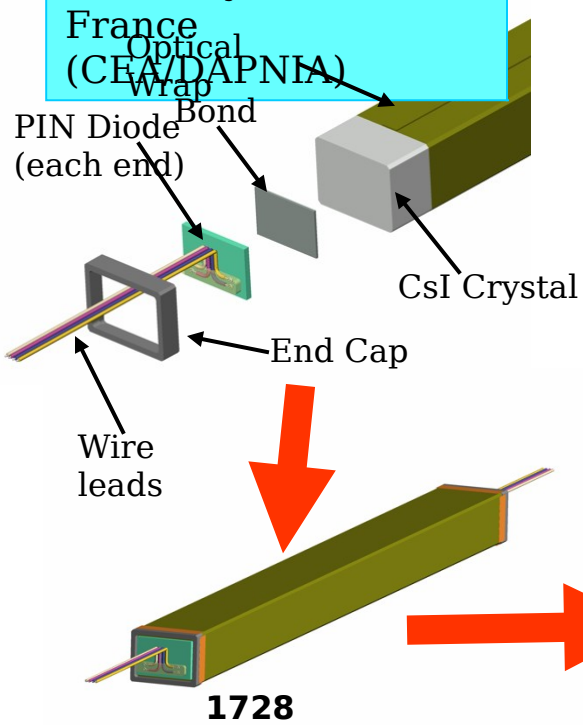
- Electronics boards attached to each side
  - Interface connectors to TEM at base of calorimeter
- Outer wall is EMI shield and provides structural stiffness as well

Calorimeter Assembly Flow

Dual PIN Diodes (DPD) NRL/CEA

CsI Crystals Sweden (KTH)

Crystal Detector Element (CDE) Assembly France (CEA/DAPNIA)



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Mechanical Structure France (IN2P3/Ecole Polytechnique)

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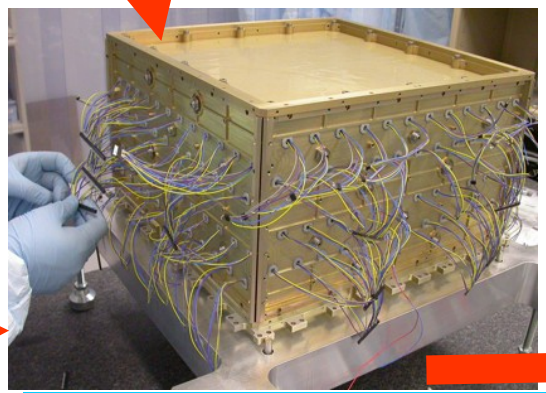

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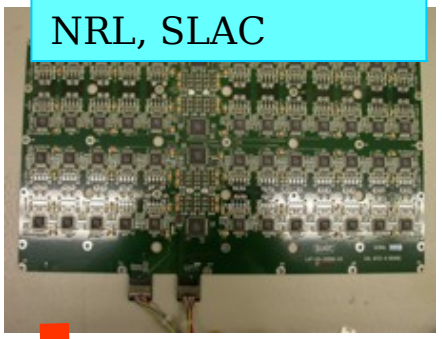
PreElectronics Module (PEM) Assembly NRL

Front-End Electronics NRL, SLAC



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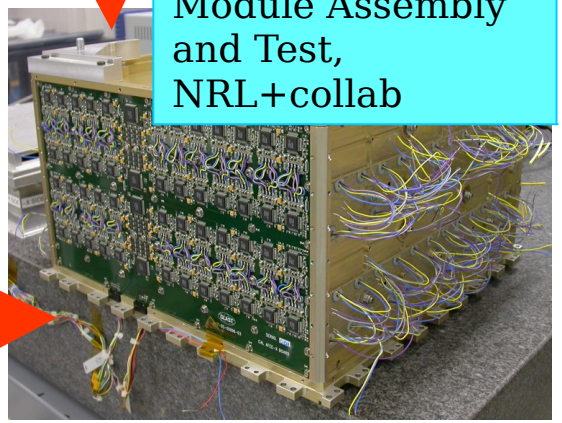
Module Assembly and Test, NRL+collab



16 Flight modules + 1 Qual + 1 Spare

Changes since Delta PDR

- Interconnect between CDE PIN diode and the Analog Front End board has been changed from flex cable to 4 28-gauge wires.
  - Presented at Delta PDR as a likely change.
  - Provides improved AFEE card layout for low noise performance.
- The Dual PIN Photodiode optical window encapsulant has changed from hard epoxy to silicone resin.
  - Unsuccessful in resolving thermal cycling stresses in the DPD and the resultant cracking and delamination of the hard epoxy window.
  - New silicone resin has been tested and meets GLAST requirements. Hamamatsu has experience with it.
- Base plate tabs that interface with the LAT grid have been redesigned to reduce stiffness and resultant stresses on the bolted joints.
- Hard mount of TEM to CAL base plate using titanium posts

CAL Peer Review

- Design maturity, qualification and verification planning near CDR level? Yes.
- Identified open design issues and established appropriate resolution plans to ensure closure? Generally yes on Technical. Issues:
  - Completion of the testing of the EM is needed
  - Substantial concern was expressed about the flight fabrication process:
    - Crystal transportation plan is likely to cause delays
    - flight CDE production in France seems very complex
    - the overall flight production schedule looks very aggressive
- Is the Subsystem near readiness for manufacturing? Yes.
- Has the Subsystem identified open manufacturing issues and established appropriate resolution plans? Qualified Yes. Concerns:
  - complexity of the fabrication
  - lack of experience with flight composite structures,
  - the likelihood that a number of problems will not emerge until after fabrication begins, and
  - the possibility that the latest round of ASICs will not fully function.

BOX SCORE: RFAs Assigned: 30 Responses completed: 27 RFAs Closed: 15

Requirements

Section 8

CAL Level III Key Requirements

Reference: LAT-SS-00018

Parameter	Requirement	Verification	Expected Performance
Energy Range	20 MeV – 300 GeV 20 MeV – 1 TeV (goal) 5 MeV – 100 GeV, single crystal	Simulation, Beam Tests	Required performance ~2 MeV threshold (BOM)
Energy Resolution (1 sigma)	<20% (20 MeV <E <100 MeV) <10% (100 MeV <E <10 GeV) <6% (10 GeV <E <300 GeV, incidence angle >60 deg)	Simulations and EM and LAT calib unit Beam Tests	Simulations demonstrate required performance
Dead Time	<100 μs per event <20 μs per event (goal)	Test	<19 μs per event
Low Energy Trigger High Energy Trigger	<2 μs trigger latency	Test	<1 μs
Mass	<1440 kg (90.0 kg/module)	Test	1376 kg
Power	<65 Watts (conditioned) (4.05 W/module)	Test	<54 Watts (conditioned)
Temperature Range	– 10 to +25 C, operational – 20 to +40 C, storage – 30 to +50 C, qualification	Subsystem TV Test 4 cycles, acceptance 12 cycles, qualification	Required performance

Derived Requirements

- **LAT CAL Subsystem Level IV Specification – LAT-SS-00210**
  - **Contains 164 detailed design requirements derived from CAL Level III Specification – LAT-SS-00018**
- **LAT CAL Verification & Environmental Test Plan – LAT-SS-01345**
  - **Details approach to verifying each Level IV requirement**
    - **Lists verification methods used**
      - **Mostly verified by Test, 53 reqmts verified by analysis/inspection**
    - **Assembly levels at which verification is performed**
      - **114 requirements are verified at the components level**

Additional details in Appendix A.

CAL Design Overview

Section 8

CAL Module

- 8 layers of 12 CsI(Tl) crystals
  - Crystal dimensions
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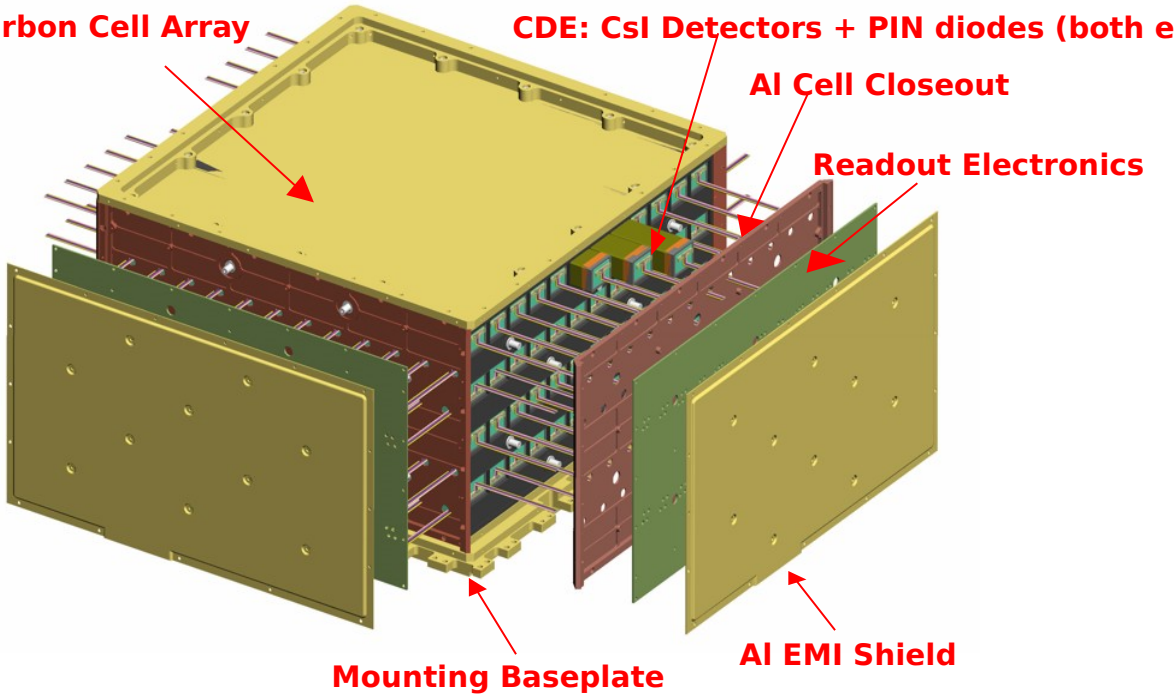
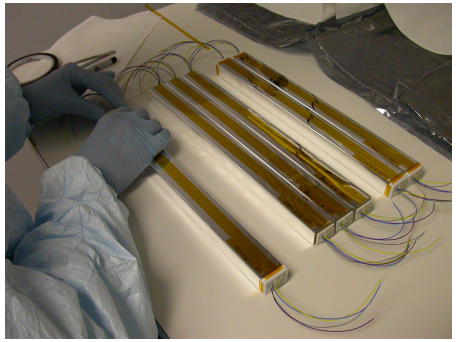
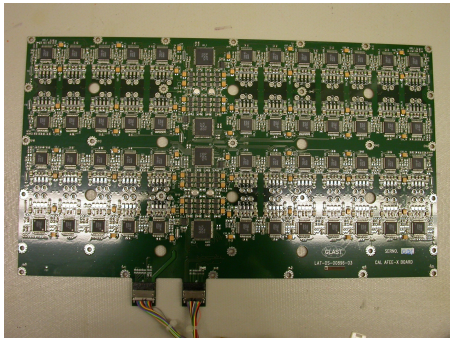


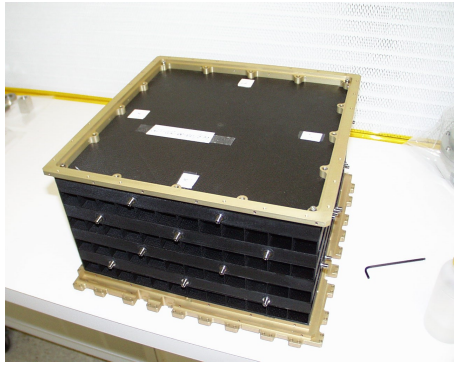
- Electronics boards attached to each side
  - Interface connectors to TEM at base of calorimeter
- Outer wall is EMI shield and provides structural stiffness as well

Concept Implementation

- **Crystal Detector Elements (CDEs)**
  - Highly segmented
    - No individual packaging: reject NaI(Tl), use CsI(Tl)
    - CsI(Tl) read with photodiodes gives ~ same light yield as NaI(Tl)
  - Photodiode readout
    - Small, lightweight, low power, rugged
    - Redundant readout gives fault protection and positions within each CsI xtal
- **Electronics**
  - Large channel count requires low power per channel, ASICs
  - Large dynamic range (~10^5) is demanding
  - Low deadtime requires COTS ADC for each channel
  - Need to minimize space, passive/empty volumes
- **Mechanical**
  - Carbon structure gives stable dimensions and fixture of detectors over thermal range and against launch loads
  - Supports detector readout on each side face of CAL







Crystal Detector Element

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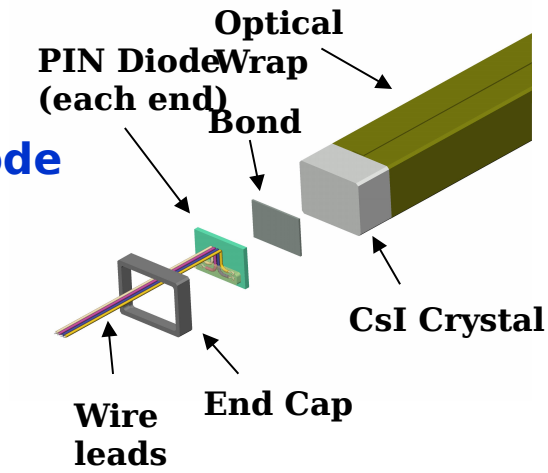
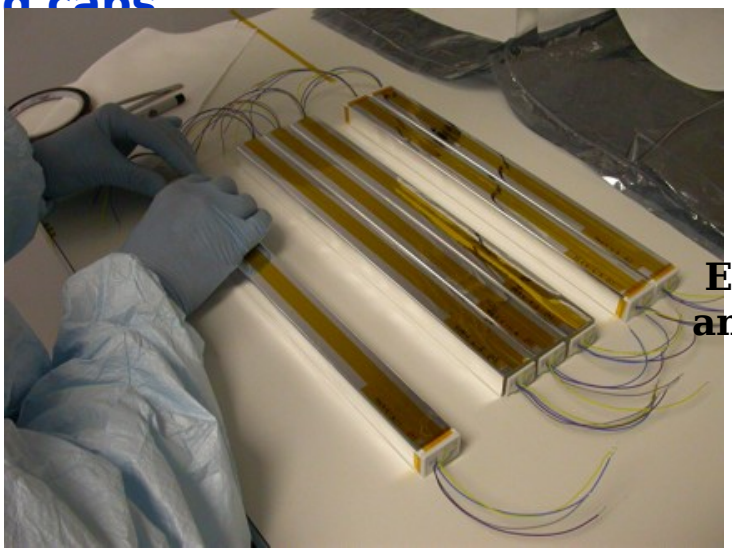
CDE Components

- **CDE has four components**
  1. CsI(Tl) crystal
  2. Two PhotoDiode Assemblies (PDAs)
     - Hamamatsu S8576-01 Dual PhotoDiode (DPD)
     - Wire leads, soldered and staked
  3. Wrapper
     - 3M Visual Mirror VM2000 film
  4. Two end caps





EM CDEs during wrapping and attachment of end caps

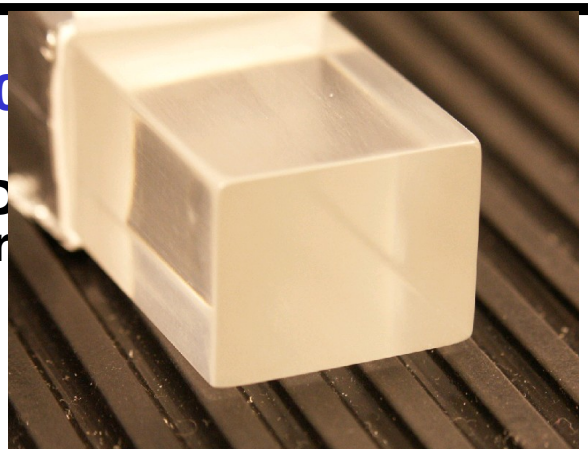
CDE Design Drivers

CDE Specification: LAT-SS-01133-02

Design Feature	Design Driver
CsI(Tl) crystal	Active calorimeter over broad dynamic range Low energy threshold High stopping power for EM showers
Crystal surface treatment (light taper)	Position sensitivity Reliable energy measurement
Photodiode readout	Low-power, low-mass, small, reliable readout High light yield (= low E threshold) with CsI(Tl)
Two dual photodiodes	Large dynamic range Redundancy for energy measurement Position measurement
VM2000 wrapper	High light yield (= low E threshold) Stable wrap, easy to handle
End caps	Stable attachment within cell

CsI(Tl) Crystal Design Drivers

CsI Performance spec: LAT-DS-00820-C



- **CsI(Tl) gives high light yield with PD good stopping power for EM shower**
  - **1536 crystals or ~1200 kg of CsI, each 326 mm x 26.7 mm x 19.9 mm**
  - **100% inspection and test**

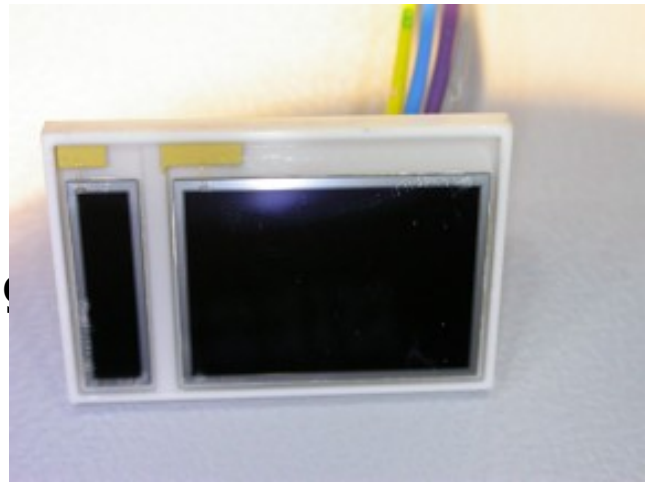
	Issue	Requirements / Comments
Mechanical	Dimensions and tolerance	Flatness of surfaces, parallelism of opposing surfaces, perpendicularity of adjacent surfaces
	Surface treatment	Polished surfaces with treatment for required light taper along crystal's length
Optical Performance	Light yield	Measured with Swedish provided test bench w/ Swedish test procedure.
	Light yield uniformity	All crystals must have same yield +/- 10%
	Light taper	End – to – end light collection requirement
	Radiation Hardness	Verified on boule samples prior to manufacture of crystals from the boule. Sweden does the test
Shipping and Handling	Shipping	Containers, environmental protection, tracking and data records
	Inspection and Tests	Acceptance testing, process control, quality provisions
Quality Control	Traceability	Amcrys-H process control and data records

Dual PIN Photodiode Design Drivers

Spec: LAT-DS-00209-12

- Spectral response well matched to CsI(Tl) scintillation
  - Very small mass, volume, and power
  - Total 3072 required in LAT CAL
  - Requirements
    - Capacitance
    - Dark current
    - Photosensitivity
    - Radiation hardness
- Two diodes to help cover dynamic ran
  - Single carrier for easier mounting
- Procurement is joint responsibility of CEA/Saclay and NRL
- Qualification, testing and processing is responsibility of CEA/Saclay
  - Lead for testing at CEA is Philippe Bourgeois

EM dual photodiode

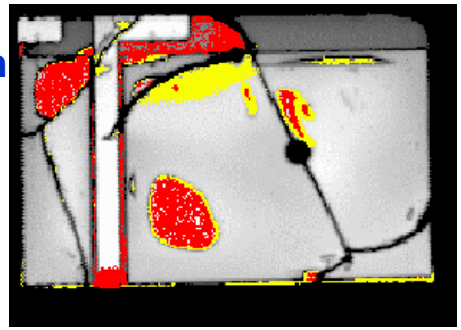


Changes from EM to Flight DPD

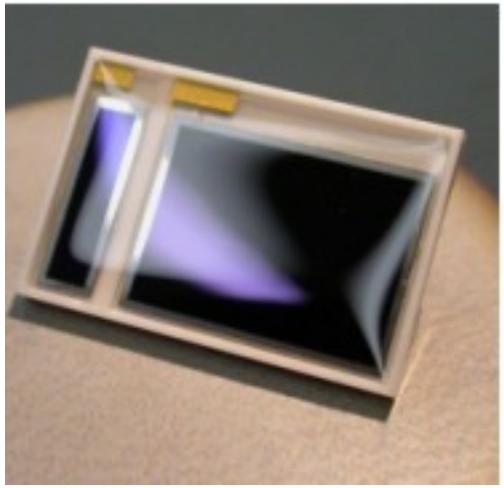
- **Several changes have been made based on EM lessons**
  - **Ceramic carrier size: S8576-01 carrier is 1 mm smaller in width and length**
  - **PIN B silicon die active area: S8576-01 die is 0.5 mm smaller in one dimension (~3%)**
  - **Electrical lead positions have been moved**
  - **Electrical leads shall be tinned by Hamamatsu prior to assembly of the silicon die to the carrier**
  - **Optical window encapsulant is changed to Shin Etsu KJR 9022E silicone resin**
  - **Shipping container has been modified to provide ESD protection and to protect the electrical leads from bending**

Dual PIN Photodiode Optical Window Issues

- **The problem with EM**
  - Hard epoxy window of EM S8576 could not withstan thermal cycling (-30C to +50C, 100 cycles)
  - But otherwise it worked well
- **The solution for FM**
  - Make the window flexible: ShinEtsu silicone
- **Verification program for ShinEtsu window: Report LAT-TD-1476-01**
  - Thermal stability of window
    - No cracks or delam at up to 180 cycles
  - Out-gassing – GSFC approved w/ bakeout
  - Bond compatibility
    - Forms fully-cured, strong bonds with optical adhesive for CsI(Tl)
  - Optical properties
    - Light yield: ~90% of hard epoxy
    - Thermal stability of optical bond: No significant loss of light after >100 cycles
  - Mechanical strength of bond
    - Tensile strength: >160 N (spec is >10 N)
    - Shear strength: >0.80 N/mm^2 (spec is >0.12 N/mm^2)



Acoustic microscopy of failed window



PDA Design

PhotoDiode Assembly Spec: LAT-DS-01534-01

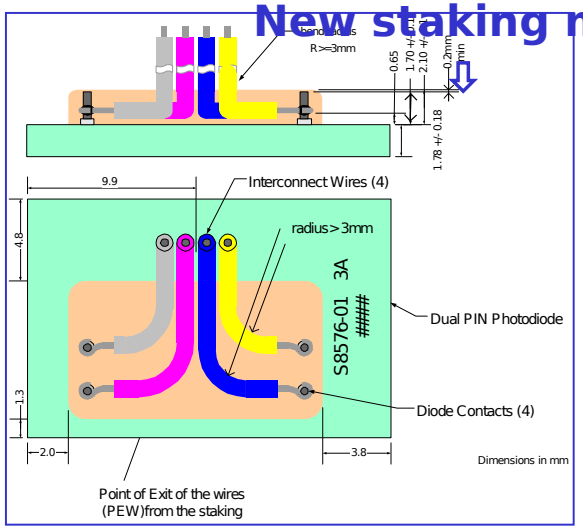
PhotoDiode Assembly: DPD + soldered wires + wires staking on ceramic

- 2 pair of 28 gauge wire for interconnect to AFEE board

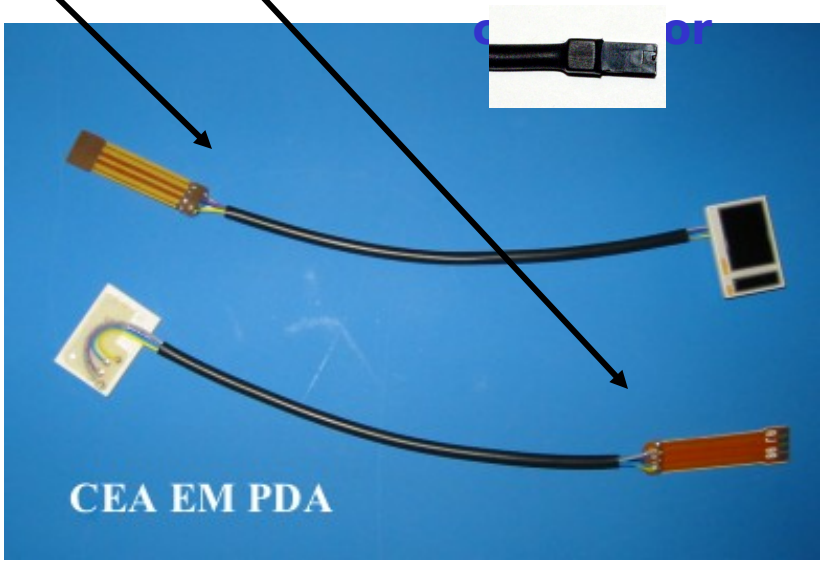
PDAfr: PDA + protective sleeve + connector for CEA test benches

New lead position of S8576-01

New staking mold

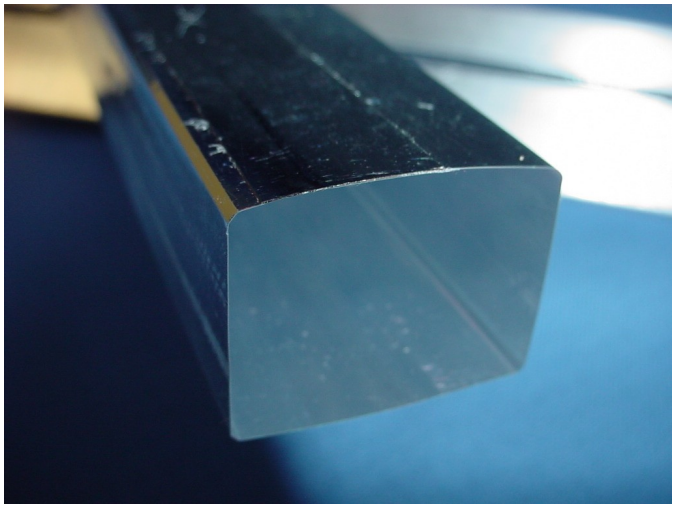


New connector



Crystal Wrapper

- **Wrapper must be highly reflective**
  - **3M VM2000 specular film**
    - **Gives 20-30% more light than standard diffusive white wraps (e.g. Tyvek, Tetratex)**
    - **Stable, rigid material will not wet xtal surface as Teflon-based wraps can (e.g. Tetratex)**
  - **Easy to form with hot molding**
    - **Form VM2000 around aluminum mandrel in xtal form (with chamfers)**
    - **No loss in light yield or mechanical stability from hot molding**
- **Procurement and molding are responsibility of CEA/Saclay**
- **Molding/wrapping procedure: LAT-PS-00795-01**

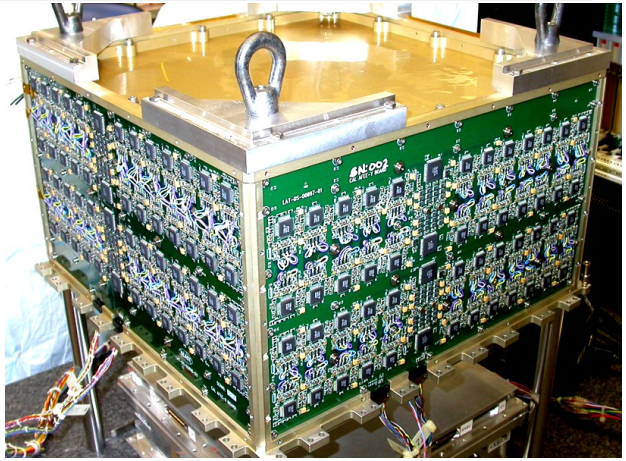


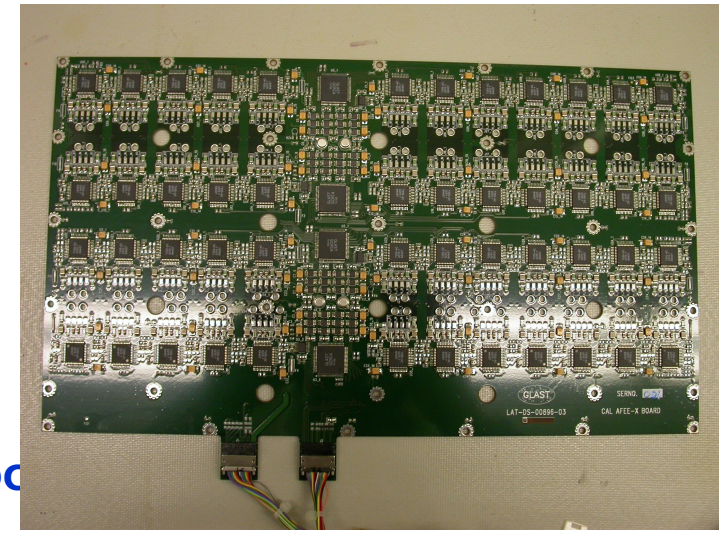
Electrical Design

Section 8

CAL Electronics Design Drivers

- **Readout both ends of CsI crystals in hodoscopic array using PIN photodiodes**
  - **4 printed circuit boards, one on each vertical face**
  - **Large dynamic range (few x 10^5)**
  - **Low noise (~2000 electrons noise)**
  - **Low power (~20 mW per crystal end)**
  - **Limited space (8 mm thickness), match pitch of CsI crystals (28x40 mm)**
  - **Interface to TEM with LAT communications protocol**
  - **Low dead time (20 μs)**
  - **Self triggering**
- **Implementation**
  - **Divide dynamic range into two input signals (dual PIN photodiode)**
    - **Each input signal goes into 2 gain ranges**
    - **Have ranges to 200 MeV, 1.6 GeV, 12.5 GeV and 100 GeV**
  - **Use 1 custom analog and 1 custom digital ASIC to minimize power**
  - **Use COTS 12-bit successive approximation ADC on each crystal end to achieve low dead time.**
  - **Sparsify data (zero suppress)**

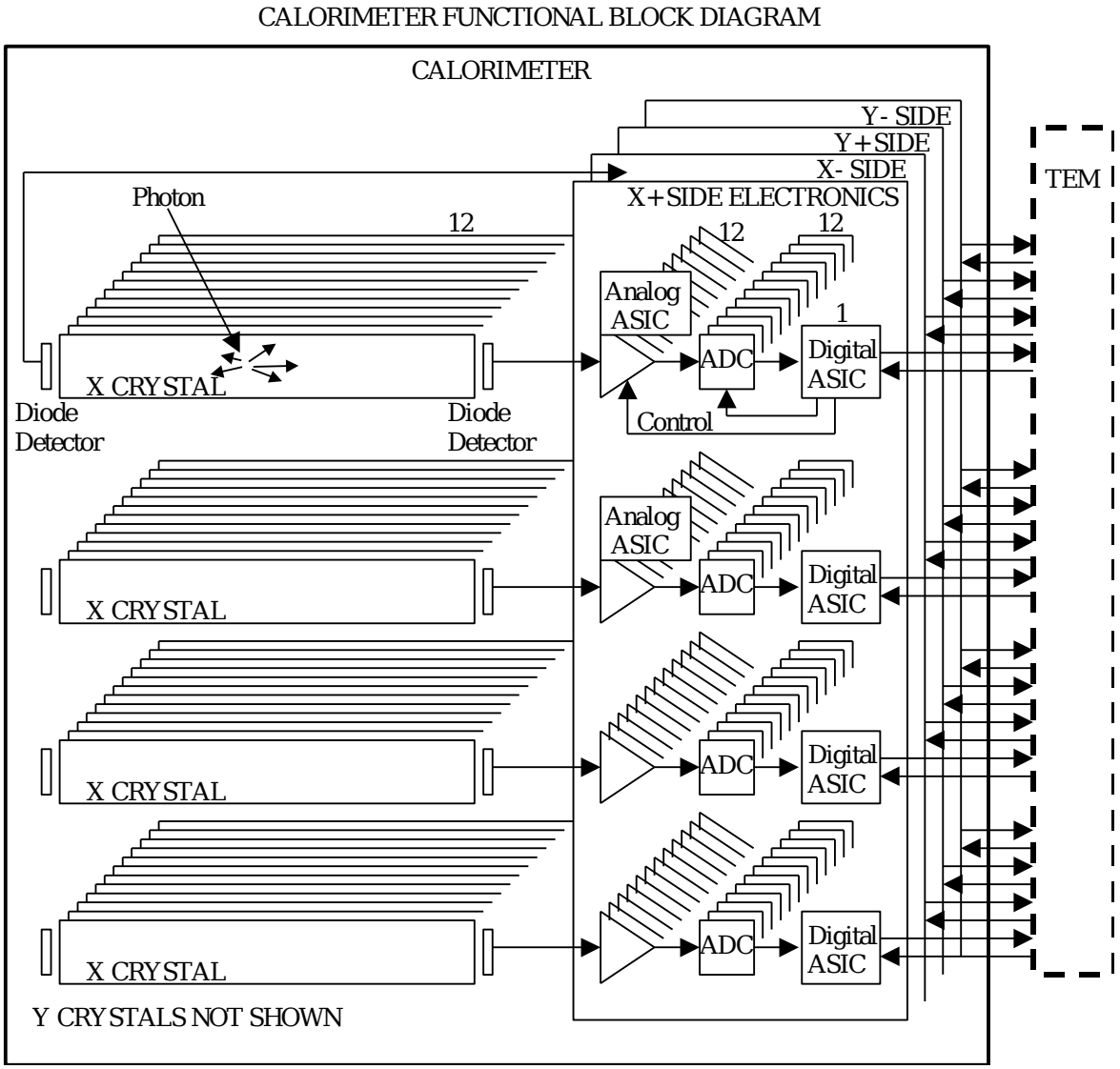




EM AFEE board

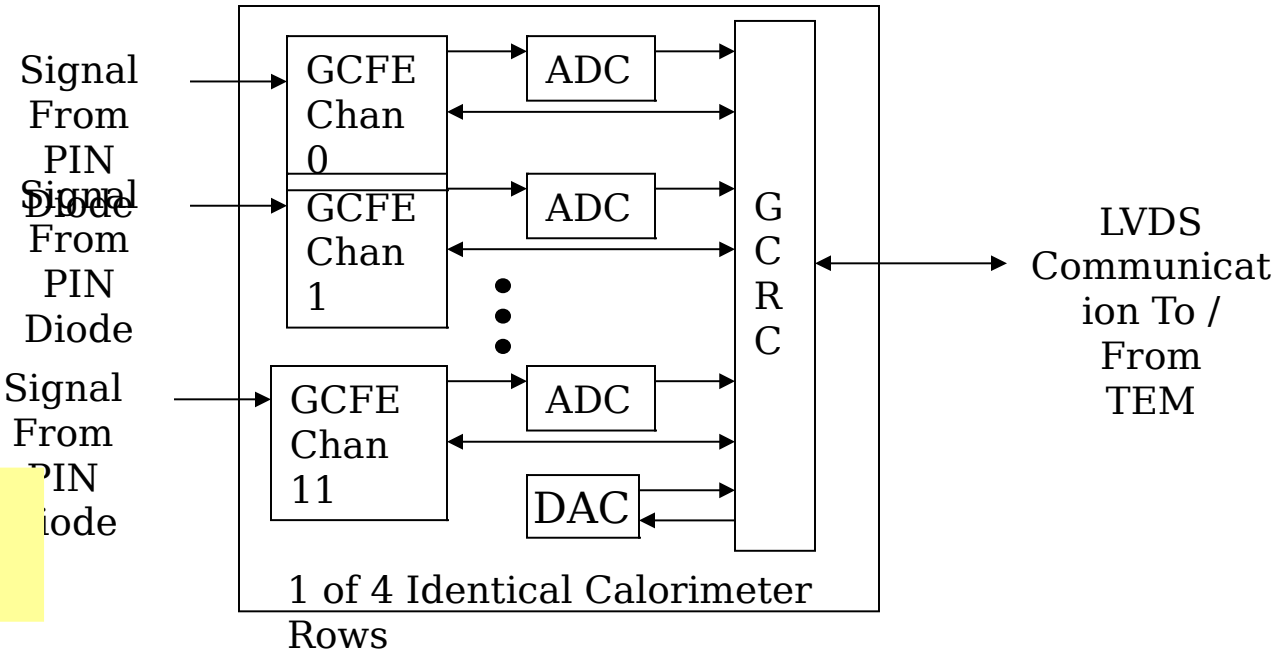
CAL Electrical Architecture

- 1 Cal electronics board (AFEE) per calorimeter side reads out 48 crystal ends.
- Each Cal circuit board communicates to Tower Electronics Module (TEM) mounted below calorimeter
- The TEM correlates crystal end readouts, zero-suppresses the AFEE data and formats the event message for the T&DF
- Redundant system, CAL can operate with loss of 1 X and 1 Y side



AFEE Design Details

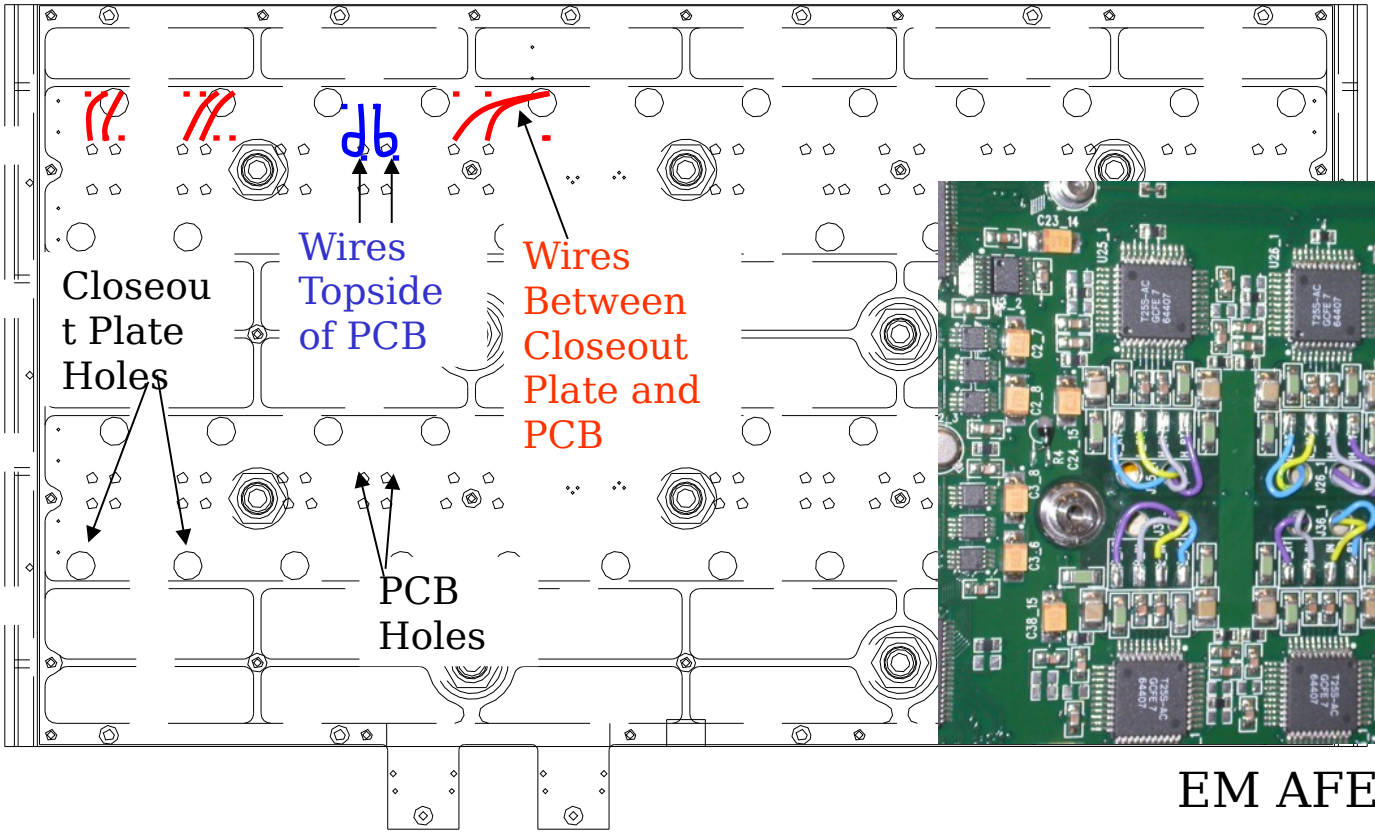
- **Cal AFEE sideboard design, electronics grouped by rows**
  - **1 analog ASIC (GCFE) and commercial ADC per log end**
  - **1 Digital ASIC per row (GCRC), communicates between GCFE - ADC pair (12 pairs per row) and external TEM**
  - **Partitioned design – communication failure of 1 GCRC only removes 1 row, short circuit failure removes 1 side board. Would still meet mission requirements**



Design: J. Ampe, NRL
Layout: M. Freytag, SLAC

PIN Diode Connection to AFEE Board

- **Plan View of EM AFEE Board PIN Diode Wiring Holes superimposed over Cal closeout plate. Few diode wire paths sketched in, representing twisted pairs**
  - **Wires staked at diode end and PCB end**
  - **Flight closeout plate to have insulating coating beneath wire runs**
  - **One rework length of wiring (5 mm) added to wire length, contained in loop on PCB**
- **Wire connection to SMT pads is labor intensive. Looking for alternatives for flight.**



EM AFEE Photo

GCFE ASIC Requirements

- **Key GCFE ASIC Requirements. From GCFE Requirements Spec, LAT-SS-00089-02, Jan 01**
  - **Total Energy Dynamic Range: 2 MeV to 100 GeV**

GCFE Range	LEx8	LEx1	LE Fast Shaper	HEx8	HEx1	HE Fast Shaper
Energy Range	2 MeV – 200 MeV	2 MeV- 1.6 GeV	2 MeV – 400 MeV	100 MeV- 12.5 GeV	100 MeV- 100 GeV	100 MeV– 100 GeV

  - **S… connected to PIN diode**
  - **Fast shaper output noise less than 3000 electrons RMS when connected to PIN diode**
  - **Slow Shaper peaking time 3.5 +/- 0.5 μsec.**
    - **Chip- Chip variation < 0.4 μsec**
  - **Fast Shaper peaking time 0.5 usec +/- 0.2 μsec**
  - **Self triggering with fast shaper discriminator**
  - **Integral non-linearity < +/- 0.5% of full scale, over 99% of energy range**
  - **Autorange energy measurement**
  - **Zero suppression flag for data sparsification**
  - **Insensitive to Latchup and total dose effects**

Design: D. Freytag, SLAC

GCFE v9 Preliminary Test Results

GCFEv9 Testing is in Progress:

- **Version 9 Known Performance Issues:**
  - **Linearity**
    - **LEx1 range measuring +/-2% Integral linearity. Can be calibrated out. Not a significant problem.**
  - **Internal DAC bias shift from shaper pedestal limits trigger efficiency for ground testing w/ cosmic muons and radiation sources.**
    - **Can be corrected with external bias resistor (to be tested).**
    - **Does not impact flight use of triggering**
- **Previous Problems Corrected in GCFE Ver 9:**
  - **Analog Output signal ringing corrected.**
  - **LVDS communication speed corrected by faster LVDS receiver.**
  - **Analog Output voltage range corrected by increasing output buffer gain.**

With testing to date, GCFEv9 is good for flight

GCRC ASIC Requirements

- Provide electrical interface between TEM and single AFEE board row
- AFEE row communications
  - Write to and Read from 12 GCFE chips
  - Write to and Read from 1 Digital to Analog Converter
- For Event readout
  - Control GCFE chips and ADCs
  - Combine data from ADCs, GCFE log accept bits, GCFE range bits and send to TEM
- Housekeeping
  - Detect communication parity errors
  - Save last command which generated parity error

Design: J. Ampe, NRL

GCRC Test Results

GCRCv5 Testing is in Progress

- **GCRCv5 Design Aspects Verified**
  - Sufficient communication timing margins
    - TEM to/from GCRC to/from GCFE tested correct operation to 40 MHz at room temperature.
  - Parity checking
  - Commanding from/to TEM
  - Reading / Writing to GCFE ASIC
  - Controlling and reading of ADCs
  - Programming onboard DAC
  - Merging event readout data from 12 ADCs and 12 GCFEs for transmission to TEM
- **Previous Problems Corrected in GCRCv5**
  - Insufficient timing margin in LVDS communications from GCFE improved by halving GCFE readback rate.

With testing to date, GCRCv5 is good for flight

AFEE Power

Power Estimate per AFEE

- (GCFEv9 and GCRCv5 have increased LVDS Receiver bias current)

	GCFEv 91 KHz evt rate	GCRCv 5 any evt rate	MAX1 45 ADC, 1 kHz evt rate	MAX51 21 DAC	Referen ce	Total Power per AFEE board	Total Power per CAL module
Analog per AFEE	230 mW				27.0 mW	257 mW	1028 mW
Digital per AFEE	317 mW	256 mW	2.0 mW	4.5 mW		580 mW	2320 mW

CAL Module Conditioned Power Allocation **18% margin**

	Analog 3.3 V	Digital 3.3 V	Bias 100V	Total Allocated Conditioned Power, Analog + Digital	Power Margin Analog + Digital
Per AFEE	300 mW	700 mW	16 mW	1016 mW	176 mW
Per Module	1200 mW	2800 mW	63 mW	4063 mW	705 mW

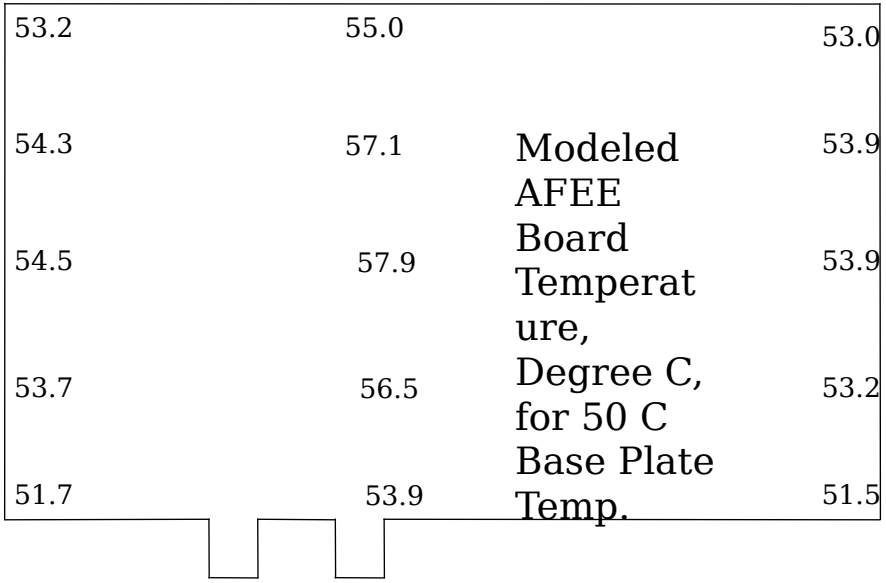
3348 mW

AFEE Thermal Analysis

- **AFEE Thermal Analysis Summary.** **From LAT-TD-01114-02 Dated 4/03**
  Author Peck Sohn, Swales Aerospace
- **Maximum silicon die temperatures for 50 C Qual Base Plate temperature**

Device	GCRC	GCFE	ADC	DAC	Ref.
Modeled Die Junction Temp. Deg. C	61.3	58.2	58.5	58.4	59.7
Maximum Derated Die Temperature, Deg. C	93	93	93	93	93

- **Analysis result, Calorimeter AFEE electronics do not have any thermal problems**



Assumptions

	Modeled Heat Dissipation	Theta Junction to Board (C/W)
GCRC	65 mW	50
GCFE	11.5 mW	114
ADC	2 mW	183
DAC	4 mW	86
Ref.	7 mW	232
Total Power per AFEE	952 mW	
AFEE PCB, Qty 2 of 1.4 mil thick Copper Thermal Plane Layers.		

Engineering Model Test Results

- **CAL EM is completely assembled and in environmental testing.**
  - **Completed comprehensive functional test and calibration**
  - **Completed Thermal cycle testing (-30 C, + 50 C)**
  - **Completed Vibration testing – Qual levels**
  - **Currently in Thermal Vacuum testing**
- **Performance meets spec with few exceptions:**
  - **Reliable LVDS communications (GCRC4-GCFE7) over temperature requires 12 MHz clock (reqmt: 20 MHz)**
    - **Known problem corrected in flight version of GCRC and GCFE.**
    - **Will not affect validity of environmental testing or science validation with EM.**
  - **Crosstalk**
    - **Calibration reference (per row) crosstalk eliminated with addition of DAC reference output capacitor.**
    - **Board level front-end cross talk still exists, assumed to be coupling through power supply. Observable ~1 MeV 'shoulders' on the muon pedestal distribution. Do not know if crosstalk can be removed by post-processing.**
    - **Other signal oddities still being examined.**

Electrical Issues and Concerns

- **Interconnect of PIN photodiodes to AFEE board needs improvements**
  - EM has good mechanical and electrical connection but the process is time consuming
  - Better routing and protection of interconnect wires
- **AFEE, GCRC and GCFE improvements for flight**
  - GCRC, GCFE: LVDS communication
    - Initial testing of GCRCv5 and GCFEv9 Looks good (40 MHz operation). Need to check margins over temperature, voltage, and total dose.
  - GCFE, AFEE: calibration signal coupling
    - Minimized w/ added DAC output capacitor
  - GCFE: Output range and ringing
    - Corrected in GCFEv9.

Mechanical Design

Section 8

Structural Analysis – Design Requirements

- Fundamental Frequency Above 100 Hz to Avoid Any Coupling with the Grid
- Min Margin of Safety = 2, For Composite Structure.
- Max Allowed Displacement for CAL Box: 0.5 mm Under Quasi-Static Loads to Avoid Any Interference with the Grid Walls
- Max Allowed Deflection of the PCBs: 0.25 mm Between Attachment Points

Structural Analysis – Tasks & Results

QUASI-STATIC AND THERMO-MECHANICAL ANALYSIS					
COMPONENT	MATERIAL	YIELD STRENGTH (MPa)	ULTIMATE STRENGTH (MPa)	MARGINS OF SAFETY	
				QUASI-STATIC ANALYSIS	THERMO-MECH ANALYSIS
Composite Structure	T300 1K/M76	-	564 (1)	21.4	1.6
Base Plate	2618A-T851	390	440	7.1	1.9
Top Frame	2618A-T851	390	440	67.7	3.0
Close-Out Plates	2618A-T851	390	440	6.7	1.4
Side Panels	5754 H111	100	220	4.9	3.1
Inserts	Ti-6Al-4V, Glass/Polyamide	-	-	4.3 (2)	0.69 (2)
PCB	Glass/Polyamide	-	89	6.5	1.9
CsI Log	Cesium Iodide	1.12	11.86	0.21	0.21

NOTES:
(1) Values Have Been Measured on Test Samples, Weave Direction
(2) Calculated for Lateral Inserts Only
(3) Analyzed to VM2 Model test Levels (20% Above Qualification) for Correlation

Structural Analysis – Tasks & Results

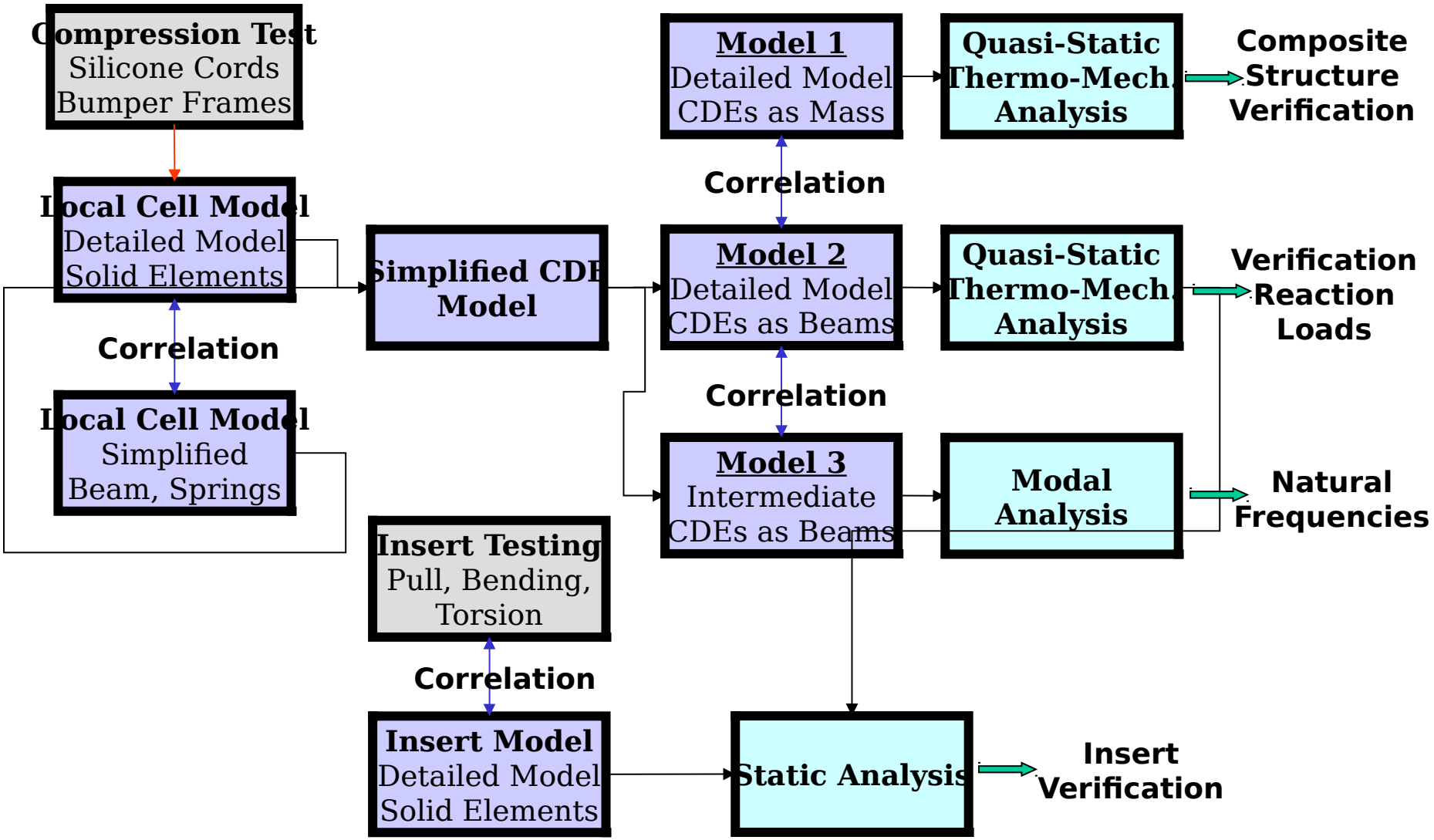
ANALYSIS TASK	RESULTS
BUCKLING ANALYSIS (1)	Bucking Factor = 15.8 (compression), 16.5 (shear)
INTERFACE LOADS ANALYSIS (2)	
Grid Interface Loading on CAL Tabs due to Limit Loads	Margin of Safety (yield) = 0.16, Factor of Safety = 1.25 Margin of Safety (ultimate) = 0.36 Factor of Safety = 1.40
Grid Interface Loading on CAL Tabs due to Out-of-Plane Distortion	Margin of Safety (yield) = 0.27 Factor of Safety = 1.25 Margin of Safety (ultimate) = 0.49 Factor of Safety = 1.40
TEM/TPS Interface Loading on CAL Base Plate	Margin of Safety (yield) = 12.0 Factor of Safety = 1.25 Margin of Safety (ultimate) = 14.0 Factor of Safety = 1.40

NOTES:
(1) Analyzed to Qualification Level Accelerations
(2) Interface Loads Analyzed to LAT Design Limit Loads

Mechanical FEA Model Description

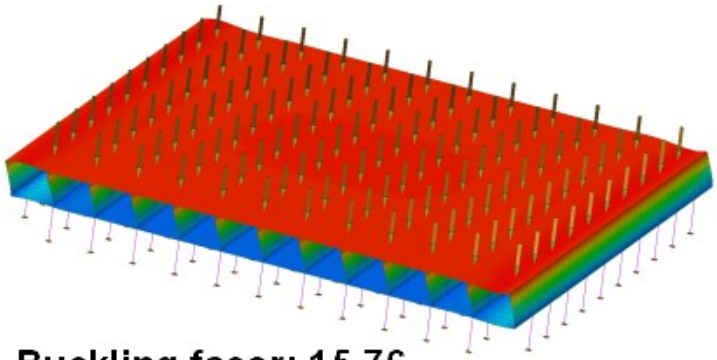
- The FEA Models of the CAL Module Have Been Built with SAMCEF V8.1 and V9 from SAMTECH. Different Models Have Been Developed to Better Fit the Analysis Needs. All Models are Correlated with Each Other.
  - Model 1: CDEs are Modeled as Structural Mass
    - Allows the Verification of the Stiffness of the Mechanical Structure without Contribution of the Crystals
    - Not Suited for Modal Analysis Because No Coupling Between the Logs and the Structure
  - Model 2: CDEs are Modeled as Beam Elements Connected to the Composite Structure and Closeout Plates by Linear Spring Elements
    - All the Connections Between the Components Have Been Included in the Model to Have Direct Information on the Reaction Loads on the Inserts and All the Fasteners
  - Model 3: Light Version of Model 2 to Perform a Modal Analysis
  - Additional FEA Modeling:
    - Local Detailed Model to Simulate the CDEs Inside the Cells and the Contribution of the Elastomeric Parts
    - Local Detailed Model to Verify the Strength of the Inserts
    - Local Detailed Models to Address Interface Aspects

Mechanical FEA Modeling



Buckling Analysis

- The Buckling of the Structure is Prevented by the Presence of the CsI Logs Inside the Cells. Still, the Composite Structure Alone Provides Enough Safety Margin
- A Local Simplified Model Has Been Developed for the Buckling Analysis of the Composite Structure. Analysis Will Be Verified on the Full Model
  - 1 Layer of 12 Cells, Model Includes Only the Composite Structure
  - Assumption of a Uniform Loading Has Been Made, Resulting From the Weight of 7 Layers of CsI Logs Under Qualification Level Accelerations
  - The Layer is Supported where X and Y Horizontal Walls Intersect
  - The Analysis is Limited to Linear Buckling, Assuming Perfect Geometry



Buckling facor: 15.76

MODES	BUCKLING FACTORS	
	Compression	Shear
1	15.8	16.5
2	21.8	-16.5

The First Buckling Mode (Compression) is Global. All the Others are Local Buckling Modes of the Inner Vertical Walls

Insert Verification

- **FE Models of the Inserts Have Been Developed and Correlated with the Test Results**
  - **Solid Mesh**
  - **Static Linear Analysis**
    - **The Reaction Loads on the Inserts Have Been Recovered from the CAL Structural Analysis. They Have Been Applied on the Local Model of the Lateral Inserts, which are the More Critical Ones.**
    - **To Reduce the Load Cases (10 Inserts Per Side, 4 Static Loads, 2 Thermal Loads), the Analysis Has Been Made for the Insert with the Max Bending Load and Max Shear Load.**
- **Analysis Show Good Correlation with the Tests Results**
  - **Failure Mode is Correctly Predicted by the Models**
  - **Margins of Safety Always >0 With 75% of the Test Failure Load**
  - **Margins of Safety Always <0 With 100% of the Test Failure Load**
- **Testing Shows Higher Failure Loads Than Analysis**

Structural Design Status

- Design Meets Strength and Stability Requirements
  - Positive Margins Have Been Calculated for All the Components
  - Displacements Are Within Acceptable Range for All the Components
- Structural Environment Testing Complete for EM (Modal Frequency Identification, Random Vibration, and Sine Burst)
  - Fundamental Modal Frequency 180 Hz
- FE Models are Currently being Correlated with Test Results from the EM Cal Module Structural Environmental Test.
- Detailed FE Model Has Been Translated from SAMCEF to NASTRAN (NASA-GSFC Deliverable)
- Independent Review of Analysis Needs to be Completed

Thermal Design

Section 8

Thermal Design Drivers

- A Total of 4 W Maximum is Dissipated from the CAL Electronics (1 W per AFEE Card) – Defined by AFEE Card Thermal Analysis
- Majority of TEM Power Dissipated to the X-LAT Plate by Thermal Straps.
- Survival Temperature Requirement Driven by Dual Pin Photodiodes
- Survival Limit Cannot be Exceeded in Test

Thermal Analysis

- **Tasks**
  - **Detailed Model of CAL Module**
    - Construction of the Detailed Model Reflecting Actual Design
    - The Detailed Model Parameters Will Be Updated According to the Thermal Balance Test Measurements on the Engineering Module
  - **Detailed Model of AFEE Card – summarized in Design - Electrical**
  - **Simplified Model of CAL Module**
    - Correlation of Results With Detailed Model
    - Delivered to SLAC
- **Methodology**
  - **Static Analysis**
    - Adjustment of the Conductances of the Simplified Model to Correlate the Results with the Detailed Model for the Hot and Cold Environment Cases
  - **Transient Analysis**
    - 10°C Temperature Step Applied on the Grid: Verification of the Correlation Between the Simplified and the Detailed Model

Thermal Model Description

- No Geometric Model
- Math Model (Not SINDA): Electrical Analogical Model Using the Orcad Pspice Simulation Software:
  - Voltage (Volt) ⇔ Temperature T (°C)
  - Current (Ampere) ⇔ Power P (W)
  - Electrical Resistance (Ohm) ⇔ Thermal Resistance (°C/W)
  - Electrical Capacitance (µF) ⇔ Thermal Capacitance Cth (J/°C)
  - Time (µS) ⇔ Time T (S)
- Simplified Thermal Model Simulation
  - Consists of 15 Nodes
  - Used for the Detailed LAT Thermal Model Simulation
- Detailed Thermal Model Simulation
  - Consists of 3150 Nodes
  - Objectives:
    - Temperature Static Analysis in the Hot and Cold Cases
    - Temperature Transient Analysis: Determination of the Build-up Time (CsI(Tl) Logs, Aluminum Plates, AFEE Boards)
    - Determine the Parameters Which Was Used for the Simplified Thermal Model

Thermal Analysis Results

Static Results – Good Correlation

HOT CASE

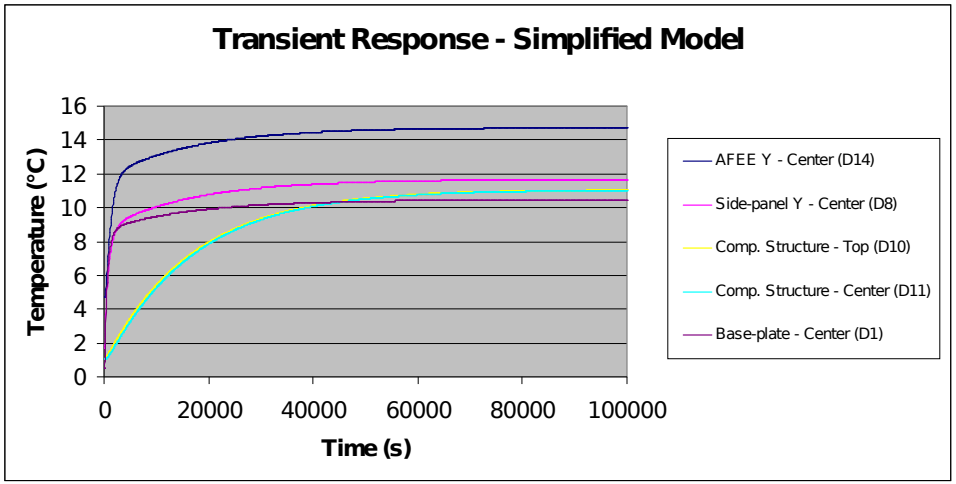
Location	N° Node	TEMP Ta (°C)	TEMP Tb (°C)	Ta –Tb (°C)
		Simplified model	Detailed model	
Base Plate – Center	1	18.74	18.64	0.1
Base plate –Face X+ Side	2	18.542	18.55	-0.008
Base plate –Face X- Side	3	18.542	18.55	-0.008
Base plate – Face Y+ Side	4	18.542	18.53	0.012
Base plate – Face Y- Side	5	18.542	18.53	0.012
Side panel – Center Face X+	6	19.64	19.4	0.24
Side panel – Center Face X-	7	19.64	19.4	0.24
Side panel – Center Face Y+	8	19.64	19.43	0.21
Side panel – Center Face Y-	9	19.64	19.43	0.21
Composite Structure - Top	10	19.188	19.02	0.168
CDE – Center	11	19.171	19.01	0.161
AFEE board – face X+	12	22.515	22.52	-0.005
AFEE board – face X-	13	22.515	22.52	-0.005
AFEE board – face Y+	14	22.515	22.51	0.005
AFEE board – face Y-	15	22.515	22.51	0.005
Grid	grid	18	18	0
TEM	tem	34	34	0
Tracker	tracker	18.5	18.5	0

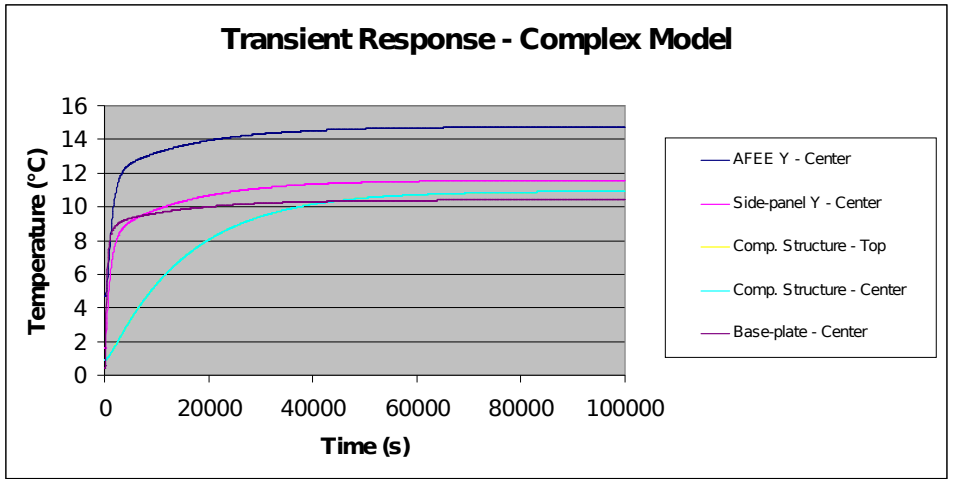
COLD CASE

Location	N° Node	TEMP Ta (°C)	TEMP Tb (°C)	Ta –Tb (°C)
		Simplified model	Detailed model	
Base Plate – Center	1	-14.52	-14.57	0.05
Base plate –Face X+ Side	2	-14.588	-14.59	0.002
Base plate –Face X- Side	3	-14.588	-14.59	0.002
Base plate – Face Y+ Side	4	-14.588	-14.61	0.022
Base plate – Face Y- Side	5	-14.588	-14.61	0.022
Side panel – Center Face X+	6	-13.483	-13.72	0.237
Side panel – Center Face X-	7	-13.483	-13.72	0.237
Side panel – Center Face Y+	8	-13.483	-13.69	0.207
Side panel – Center Face Y-	9	-13.483	-13.69	0.207
Composite Structure - Top	10	-14.024	-14.15	0.126
CDE – Center	11	-14.041	-14.15	0.109
AFEE board – face X+	12	-10.608	-10.6	-0.008
AFEE board – face X-	13	-10.608	-10.6	-0.008
AFEE board – face Y+	14	-10.608	-10.4	-0.208
AFEE board – face Y-	15	-10.608	-10.4	-0.208
Grid	grid	-15	-15	0
TEM	tem	-11	-11	0
Tracker	tracker	-17	-17	0

Thermal Analysis Results

- **Transient Results – Good Correlation**
  - **A 10°C Temperature Step was Applied on the Grid in Order to Verify the Correlation Between the Simplified and Detailed Models**





Thermal Design Status

- **Detailed and Simplified Thermal Models Have Been Developed and Current Simulations Show That the Thermal Design Is Sound:**
  - **The Max Difference of Temperature Between CDEs is 0.7°C, Accounting for Max Values of Contact Thermal Resistances**
- **Independent Review of Analysis is Complete**
- **Thermal Vacuum Testing of the CAL EM is Ongoing.**
  - **Temperature Build-Up Time of the CDEs is Very Dependent on the Contact Resistances Between Parts (Aluminum-Composite, Titanium-Aluminum, CDE-Composite), which will be Verified during Test.**
  - **Both Thermal Models Will Be Updated According to the Thermal Balance Measurements**
    - **Thermal Model Update Will Only Affect the Parameter Values**
    - **Thermal Model of the Structure Will Not Change**

Design Status

Section 8

Design/Documentation Status

- 156 Documents/Drawings have been completed
  - 255 Document total includes 65+ GSE drawings, test documents, test reports, etc
  - 85% of Documentation complete to support Flight Fabrication
- Incomplete documents supporting Flight model fabrication & testing (10)
  - Flight CDE Assembly & Test Procedures incomplete
    - Documents are CEA responsibility
      - Completion date TBD
    - Engineering model procedures complete
- Design Documentation and Worst Case Analyses (WCA) for the GCFE and GCRC ASIC devices are not completed (6)
  - Necessary for AFEE Board Electrical Worst Case Analysis
    - Need by 5/24 to support AFFE Flight build
    - Documents are in progress at SLAC

Design/Documentation Status (cont)

- **Flight AFEE Board Fabrication & Board Test documentation not complete**
  - **Engineering model drawings released.**
  - **Flight model drawings are waiting for AFEE board design modification based on lessons learned from EM fabrication and test.**
  - **AFEE Board WCA requires completed ASIC characterization**
    - **Flight ASIC design analyses not complete**
    - **Flight device testing is not complete**
  - **Scheduled for completion by 6/28 to support Flight builds**

Verification Program

Section 8

Verification & Test Overview

- CAL Module concept has been developed and verified with several prototype mechanical structures and detector elements
  - VM1 (2001), LM and VM2 (2002)
- A complete Engineering Model has been constructed and is undergoing Qualification testing
  - EM is full fit, form, function of a flight module
  - EM testing is dry run for Flight Model A Qualification testing
  - Test procedures will be updated prior to FMA testing
  - EM is specially instrumented to assist thermal profiling
- Structural Model (SM) and Structural Flight Model (SFM) testing will qualify change in Composite Structure process
  - Vibration testing at Qualification levels
  - Flight structure with mass simulators for CDEs, electronics
- Qualification model (FMA) and Flight spare (FMB) are first units off flight production line
  - Qual test levels including 12 Thermal-Vacuum cycles.
- Sixteen Flight models undergo Acceptance testing
  - Vibration testing and 4 Thermal-Vacuum Cycles at Acceptance levels

Verification Matrix

From CAL Module Verification & Environmental Test Plan – LAT-SS-01345

		HARDWARE				MECHANICAL							ELECTRICAL					THERMAL				OTHER					
MODEL	LEVEL	COMPONENT (ITEM)	QUANTITY	TYPE	SUPPLIER	STATIC LOAD	SINE BURST	SINE SWEEP	RANDOM VIB	ACOUSTIC	PRESSURE PROFILE	MASS PROPERTIES	INTERFACE VERIFICATION	EMC/EMI	ESD COMPATABILITY (GRD)	MAGNETICS	FUNCTIONAL	THERMAL VACUUM	THERMAL BALANCE	THERMAL CYCLE	HUMIDITY	RADIATION	BAKEOUT	BEAM TEST-EM SHOWERS	BEAM TEST-HADRONS	BEAM TEST - HEAVY IONS	COMMENTS
	C	VM2 CsI Det Elements (CDE)	12	Q	F	A			A			M	T	A	A	A	T	TQ		TQ		T					
	C	VM2 PreElect Modules (PEM)	1	Q	F	T	TQ	TQ	TQ		TQ	M	T				T	TQ		TQ			T				
	C	VM Electronics Prototype	1	Q	N												T										
ENGINEERING	C	EM CsI Det Elements (CDE)		Q	F/N							M	T				T			TQ	M	TQ					TQ applies to sample batches
	C	EM Composite Structure	1	Q	F	TQ						M											A				
	C	EM Front End Elect (AFEE)	4	Q	N	A	A	A	A			M	T	A	A	A	T			TQ	M	A	A				
	S	**EM CAL Module**	1	Q	N		TQ	TQ	TQ		A	M	T	T	T	T	T	TQ			M	A	A	T	T	T	
STRUCTURAL																											
	S	**SM CAL Module**	1	Q	F	TQ	TQ	TQ	TQ			M											A				Structural Model
	S	**SFM CAL Module**	1	Q	F	TQ	TQ	TQ	TQ			M											A				Structural Flight Model
QUALIFICATION																											
	C	QM CsI Det Elements (CDE)		Q	F							M	T				T			TQ	M	TQ					TQ applies to sample batches
	C	QM Composite Structure	1	Q	F	TQ						M											A				
	C	QM Front End Elect (AFEE)	4	Q	N	A	A	A	A			M	T	A	A	A	T			TQ	M	A	A				
	S	**QM CAL Module**	1	Q	N		TQ	TQ	TQ		A	M	T	T	T	T	T	TQ			M	A	A				
FLIGHT	C	FM CsI Det Elements (CDE)		F	F							M	T				T			TQ	M	TQ					TQ applies to sample batches
	C	FM Composite Structure		F	F	TA						M											QS				
	C	FM Front End Elect (AFEE)		F	N	QS	QS	QS	QS			M	T	QS	QS	QS	T			TQ	M	QS	QS				
	S	**FM CAL Module**	17	F	N		TA	TA	TA		QS	M	T	QS	QS	QS	T	TA			M	QS	QS				

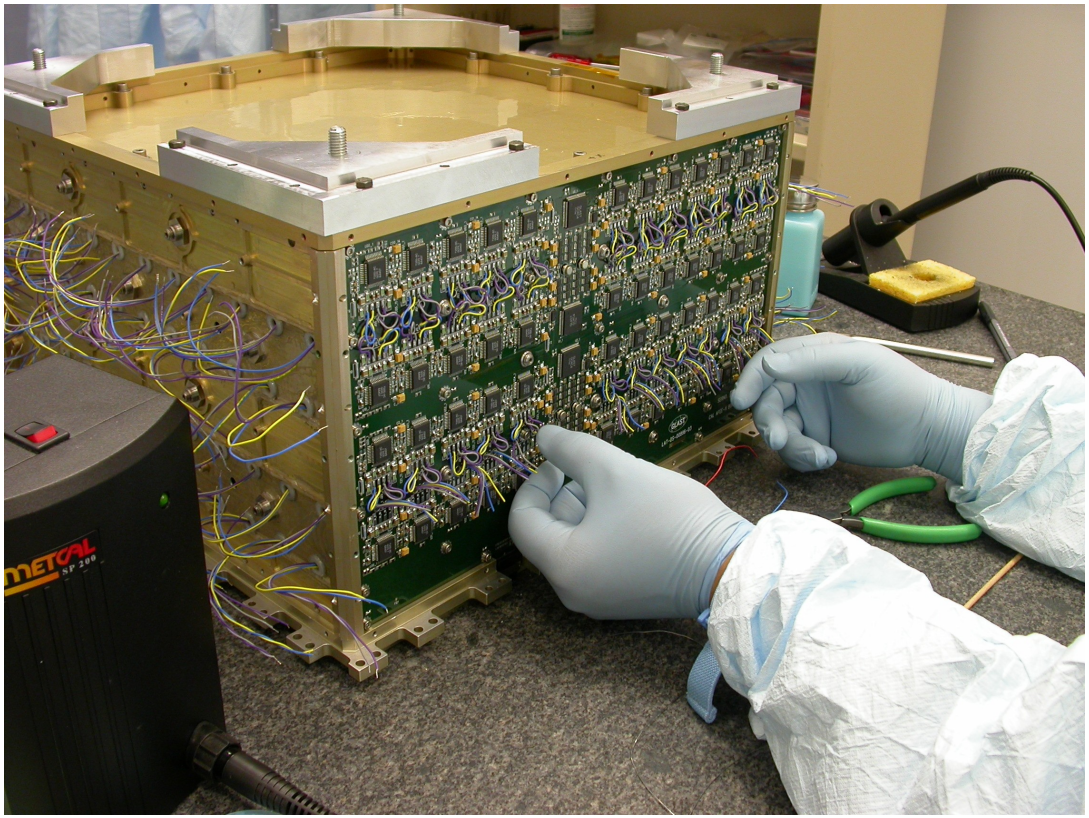
LEVEL OF ASSEMBLY:	**SUPPLIER:**	**UNIT TYPE:**	**VERIFICATION METHOD:**		
S = Subsystem	F = France	PR = ProtoFlight	T = Test	TQ = Test, Qual. Level	
C = Component	N = NRL	F = Flight	A = Analysis	QS = Qual by Similarity	
		S = Spare	M = Measurement	TA = Test, Acceptance Level	
		Q = Qualification Unit	I = Inspection		

Design Development and Verification

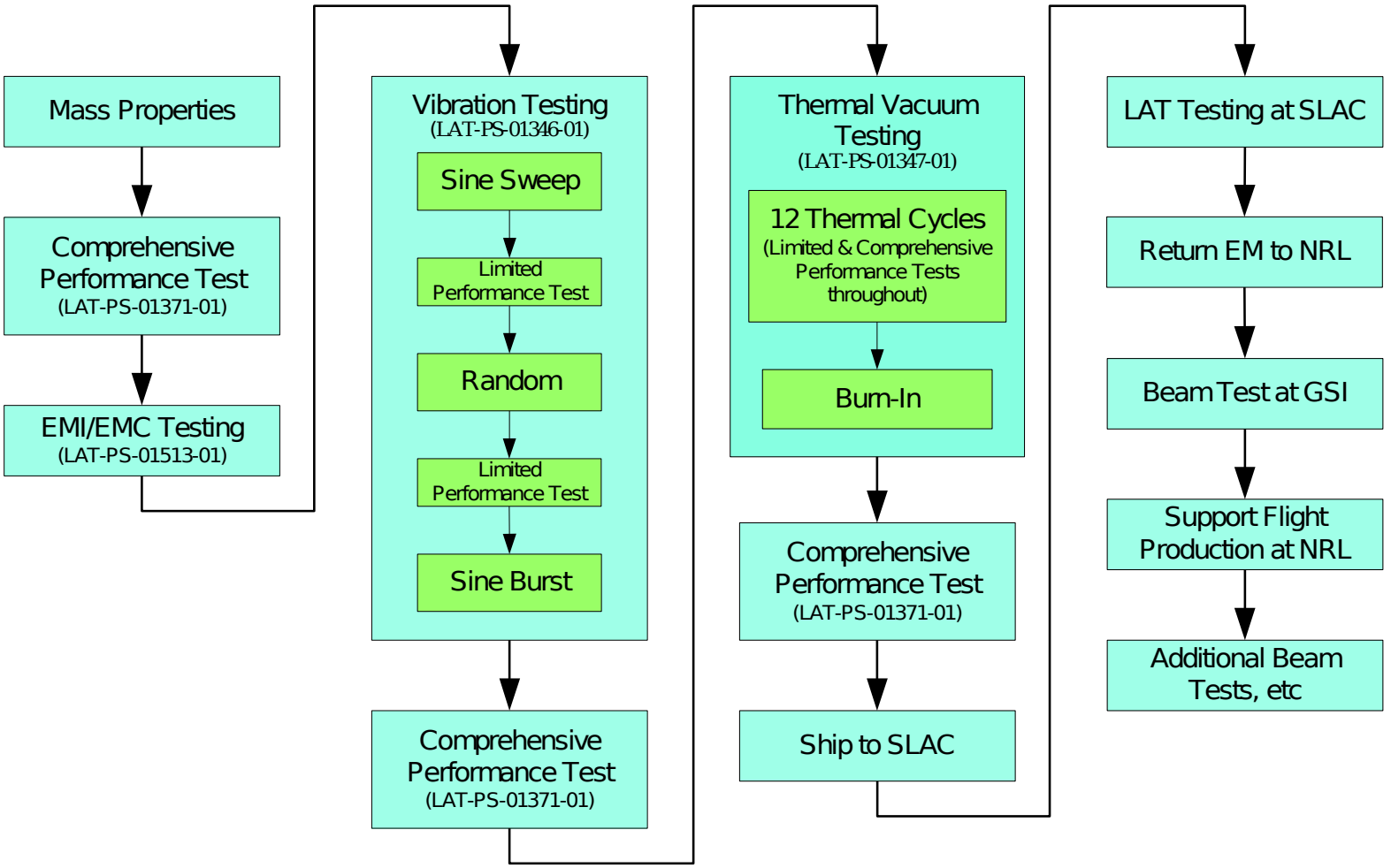
	Description	Test	Results
VM1	96 cell structure, Al shell • 93 dummy logs • 3 bare CsI logs	Vibration test • Sine sweep • Random (Qual) • Sine burst (Qual) CsI light yield	• Verified composite structure fab • Verified structure strength • Verified CsI xtal – cell interface concept LAT TD-00243-01
LM	1 layer structure 12 CDEs	Vibration test • Random (Qual) Therm Vac • (-30, +50, Qual) CDE light yield	• Verified CDE concept • Verified CDE – cell structure I/F LAT TD-00850-02
VM2	96 cell structure, Al shell • 87 dummy logs • 9 bare CsI logs	Vibration test • Sine sweep • Random (Qual + 3dB) • Sine burst (Qual x 1.2) Thermal cycling (no CDEs) CsI light yield	• Verified structure strength • Verified CDE – cell I/F • Verified EM design LAT TD-00850-02

Engineering Model

- **EM Calorimeter**
  - **Full-size calorimeter**
  - **Fully populated with CDEs and AFEEs**

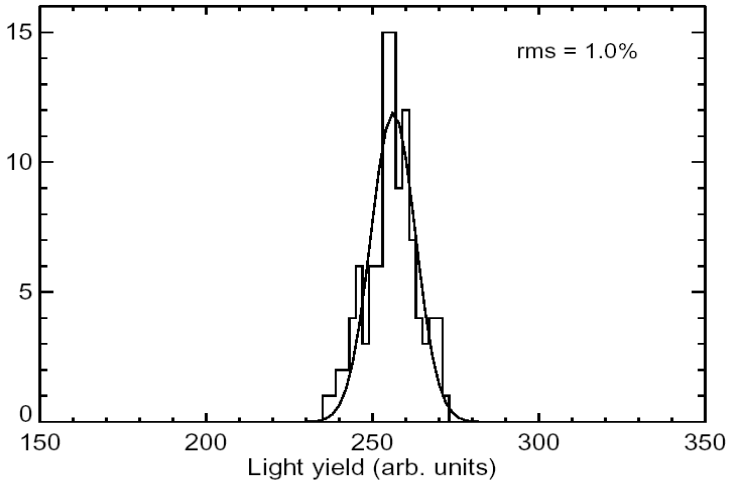


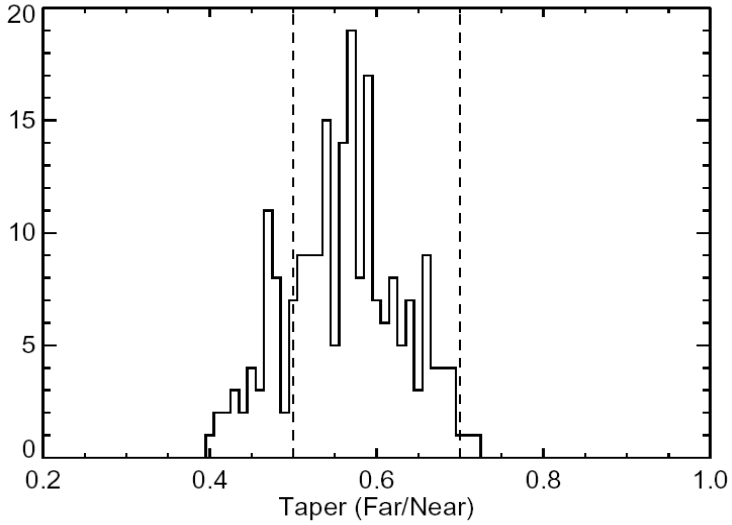
EM Verification Test Flow



EM Crystal Performance

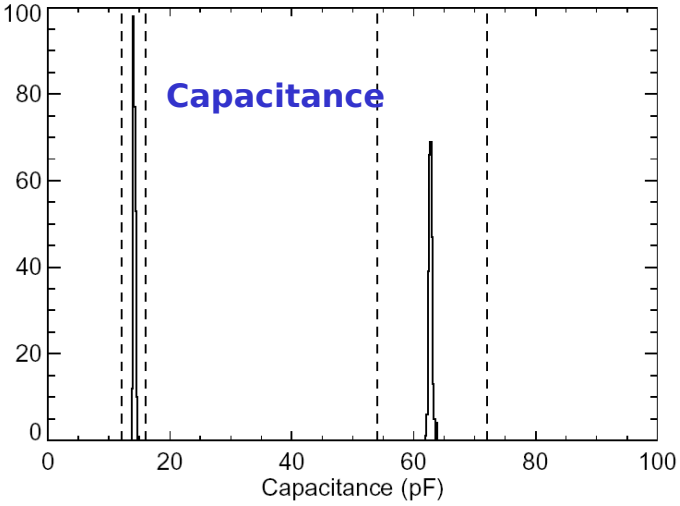
- CsI(Tl) crystals
  - Vendor: Amcrys H, procured 244 xtals
  - Dimensional specs changed
    1. Remachined length
    2. Remachined chamfers
- Results
  - Light yield constancy is within spec
  - Light taper is (mostly) within spec
  - Energy resolution is within spec

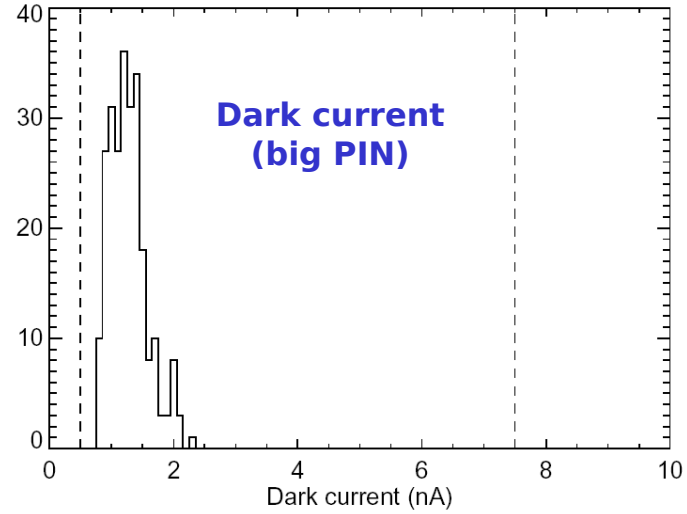




EM Photodiode Performance

- **EM photodiode**
  - Vendor: Hamamatsu, custom S8576
  - Procured 650 DPDs according to spec LAT-DS-0072-03
- **Testing**
  - Electrical performance at NRL and in France - Within spec
  - Optical performance in France - Within spec
  - Radiation hardness in France - Within spec
  - Bonding studies at NRL and in France - Within spec
  - Thermal stability at NRL and in France – Optical window material failed – Flight diode changed to silicone optical window

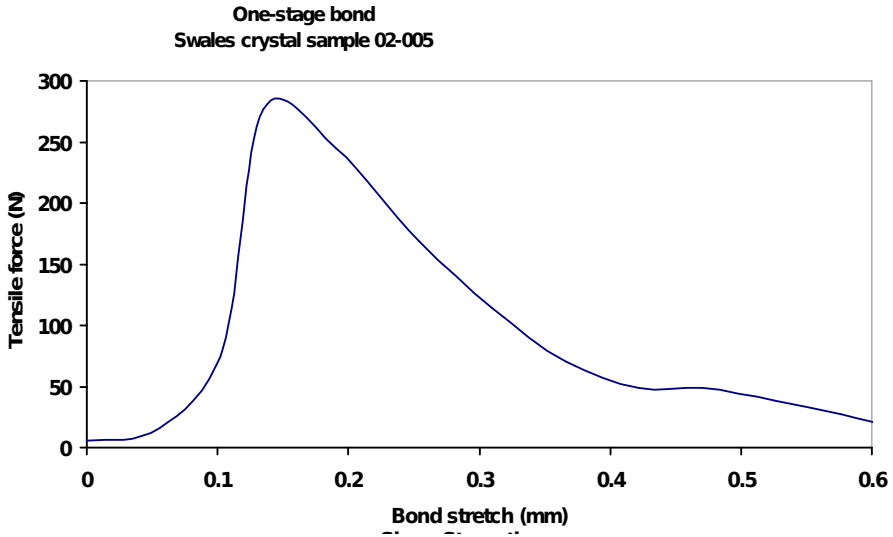


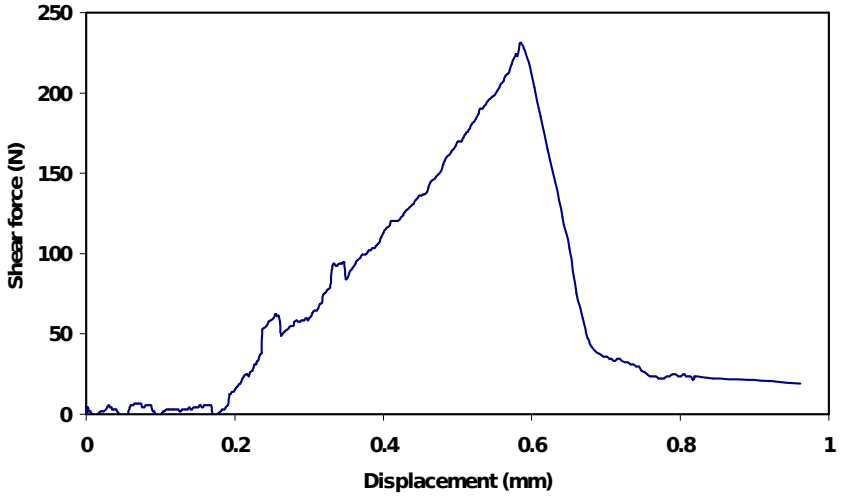


EM CsI – PIN Diode Bond: Strength Tests

- More than 65 bonds tested
  - Tensile strength sample
    - Fails at ~280 N
      ➔ 28 x requirement
  - Shear strength sample
    - Fails at ~230 N
      ➔ 7 x requirement
- Typical failures are
  - ~10 x strength requirement
  - At interfaces, rather than in bond material
    - Slightly more likely at diode face

Adhesion problem with CsI is solved



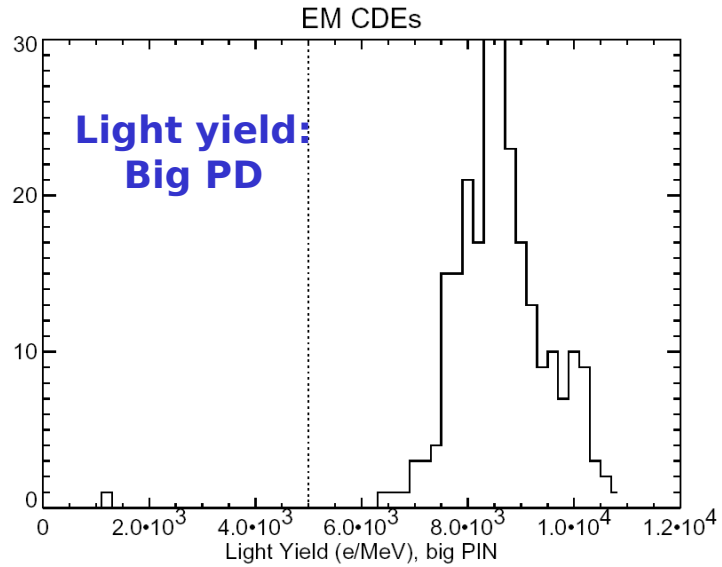


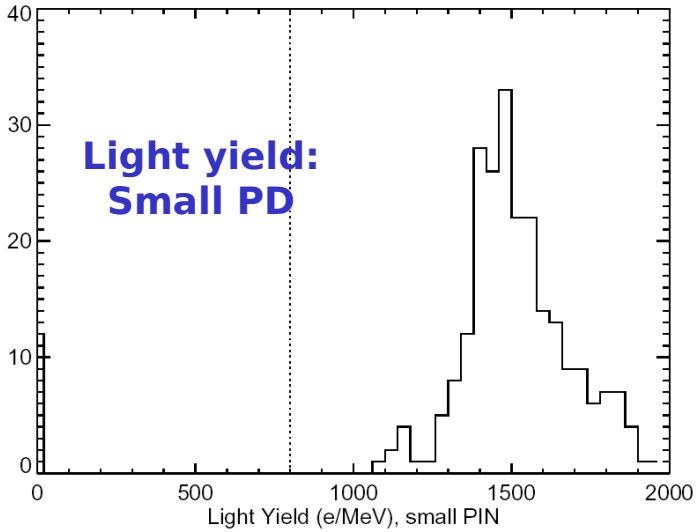
EM CDE Performance

- **EM CDE build**
  - 110 at Swales Aerospace
  - 14 at Saclay

Saclay and Swales CDEs have identical performance

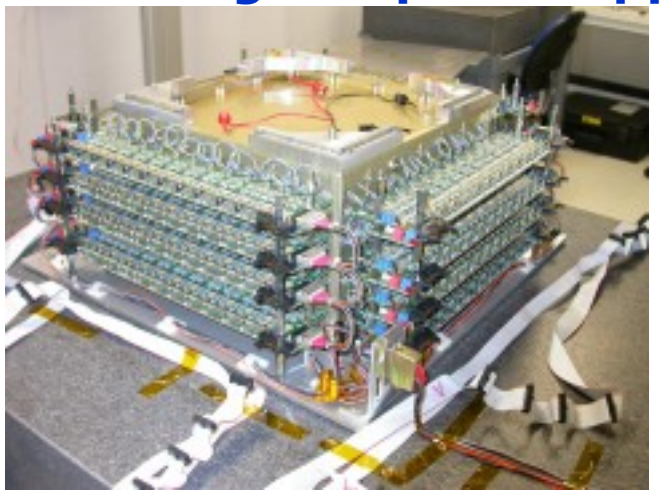
- **Performance of EM CDEs**
  - Light yield
    - Big PD within spec
      - Typical: 8000 e/MeV
      - EM Spec: >5000 e/MeV
    - Small PD within spec
      - Typical: 1500 e/MeV
      - EM Spec: >800 e/MeV
  - Light asymmetry (mostly) within spec
    - EM spec: >0.17, <0.39

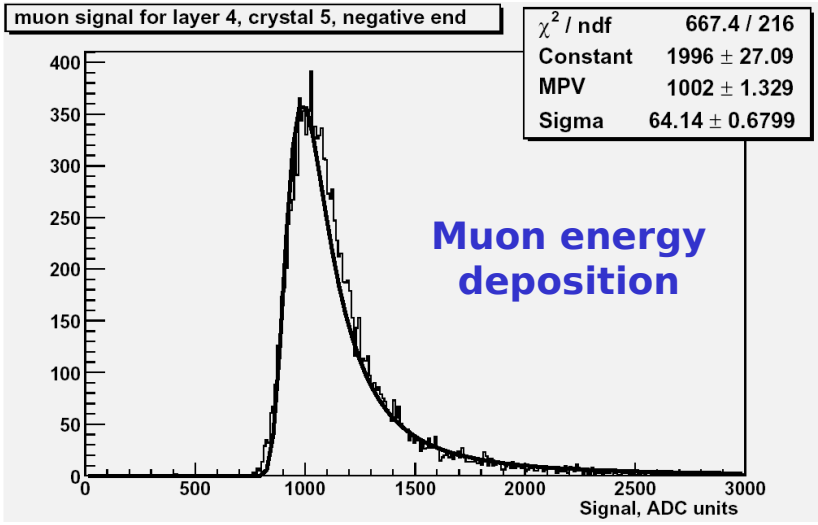


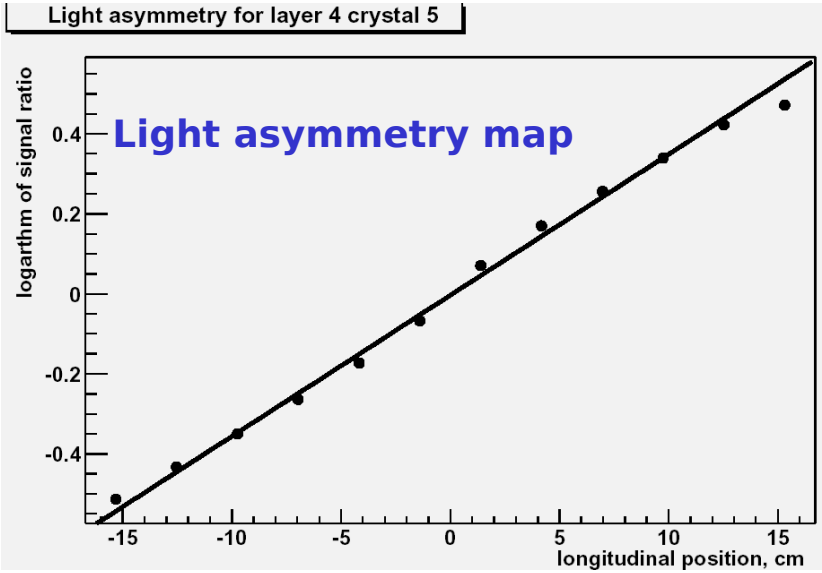


EM Pre-Electronics Module Performance

- **Performance of EM PEM**
  - Assembled PEM with GSE Checkout electronics
  - >5 million muons collected
  - Data being analyzed with Ground Science Analysis Software system
    - Muon trajectories imaged
    - CDE light tapers mapped







Fidelity of EM to FM

- Designed and fabricated to be as accurate a representation of the flight CAL module as possible
  - Principle: "Full flight form, fit and function"
  - Flight quality parts where available
- Known deviations from flight modules:
  - PIN photodiodes
    - FM DPD is smaller than EM by 1 mm in 2 dimensions, electrical connections are moved
    - FM DPD optical window has changed to ShinEtsu silicone
    - Additional tests of CsI-DPD bonding process are needed for new optical window. Initial tests are fully successful.
  - 14 of 96 EM CDEs were manufactured in France
  - ASICs
    - FM GCFE will be version 9. EM is version 7
    - FM GCRC will be version 5. EM is version 4
  - FM composite structure will use an improved (autoclaved) curing process
  - FM surface treatment on baseplate tabs may be different

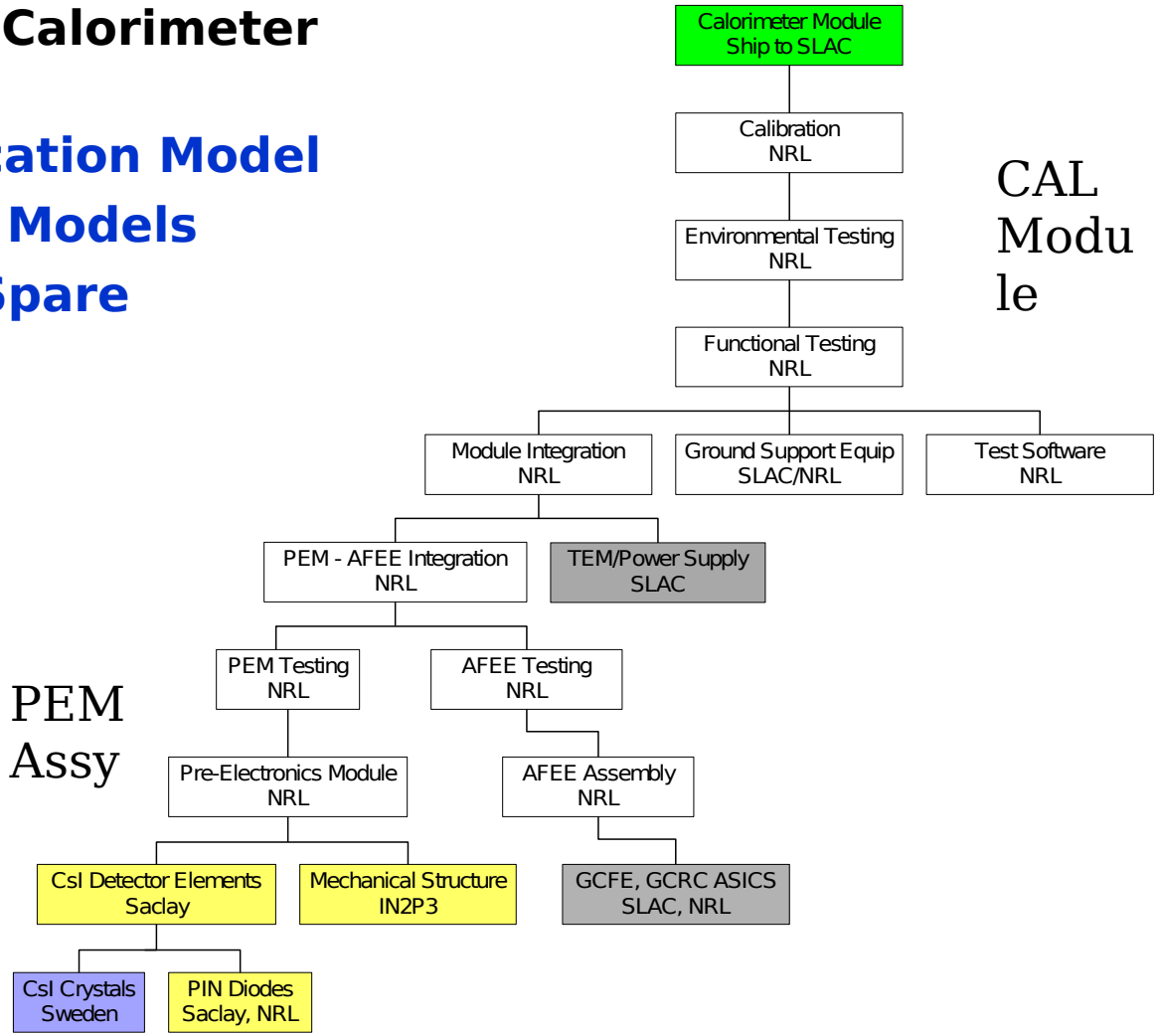
Fabrication Highlights

Section 8

Additional details in Appendix B.

Calorimeter Assembly Overview

- **18 Identical Calorimeter Modules**
  - **1 Qualification Model**
  - **16 Flight Models**
  - **1 Flight Spare**



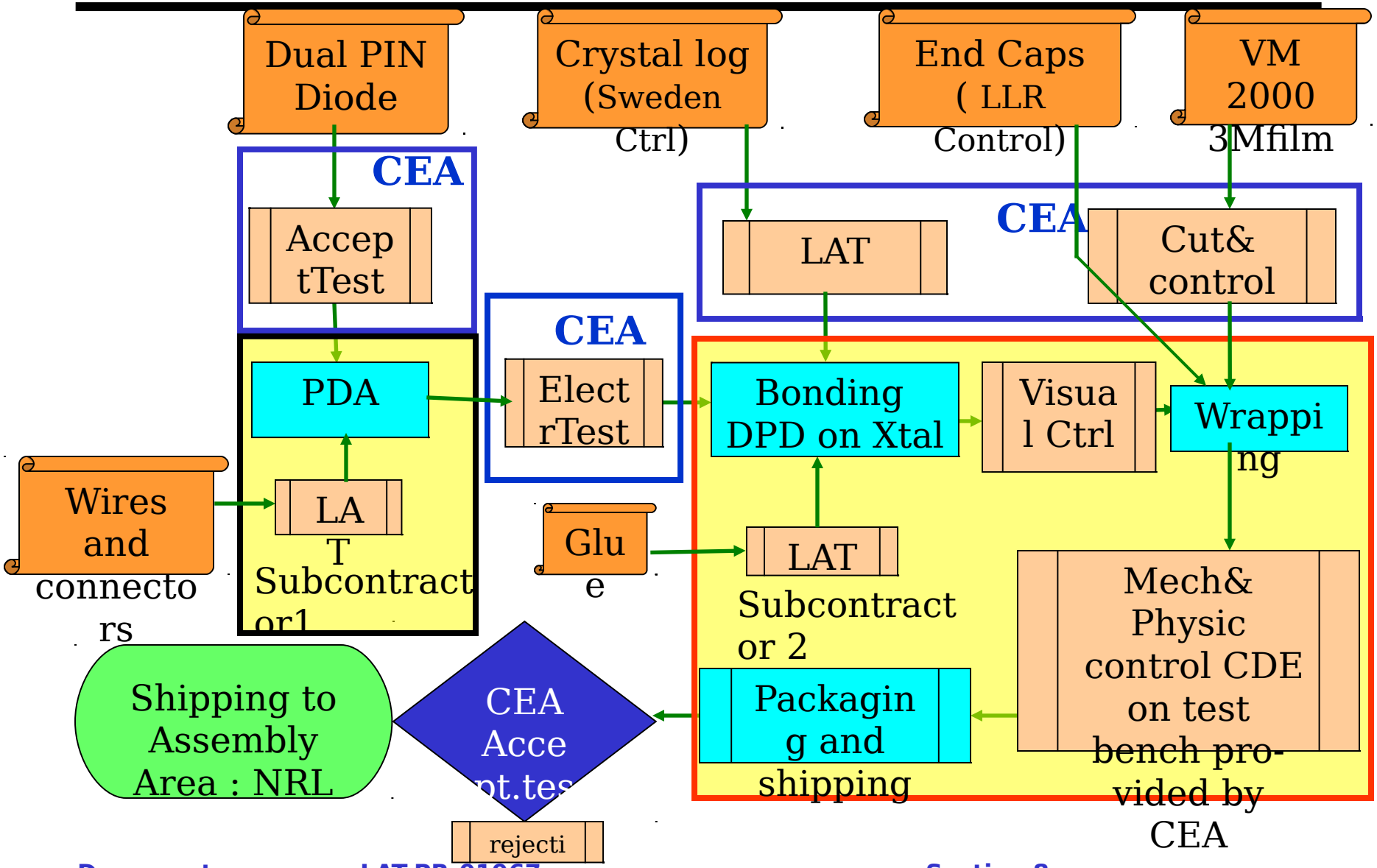
Manufacturing and Reliability

- EM program was used to define and test the processes and procedures that will be used for flight module manufacturing.
  - Configured specifications and procedures
  - All work was performed using closed-loop work order authorization where all non-conformances were recorded.
  - These procedures will be modified from the lessons learned prior to flight fabrication and testing.
- EEE Parts Control Board has approved all CAL parts except ADC, DAC, and ASICs
  - A qualification and screening program for the ADC and DAC has been approved by the PCB and is starting
  - A similar program for the plastic encapsulated ASICs is being developed with the PCB.
- All CAL materials and processes have been approved for flight by the LAT Mechanical Parts Review Board and by GSFC.
- CAL manufacturing will use approved and controlled procedures at all participating institutions:
  - Quality Assurance Implementation, LAT-MD-01472,
  - Configuration Management Plan, LAT-MD-01486,
  - Contamination Control, LAT-MD-00228.

Crystal Procurement

- Contract and procurement process by Swedish Consortium
  - Competitive selection of Amcrys-H completed in Feb 2001
  - 244 Prototype crystals delivered May 2001 – Apr 2002 for development and EM module
  - Revised specification Feb 2002 (LAT-DS-00820-03)
- Successful flight Procurement Readiness Review Feb 2003
  - First flight xtal delivery to Kalmar expected May 2003
  - Total flight purchase: 1945 xtals
- Flight Crystal Processing
  - Delivered by Amcrys-H at rate of ~ 200/month.
  - Performance verified at factory with Swedish optical and mechanical test benches
  - Acceptance testing performed in Sweden, verification and checking of data package.
  - packed and shipped to France for CDE manufacture

CDE Manufacturing Plan



CDE Manufacturing Status

- **PIN Diode Assembly – contract with industry in France**
  - **Contract award expected May 21**
  - **First deliveries (264) on Aug 8**
  - **120 PDA per week**
- **CDE bonding and wrapping – contract with industry in France**
  - **Contract award expected May 24**
  - **First deliveries (120) on Sept 10**
  - **Start at 54 CDE/week growing to 81 CDE/week**

Mechanical Structure Manufacturing - LLR

- **Metallic Parts: Aluminum Plates, Titanium Inserts and Nuts**
  - Contract with Industry, Includes fabrication, alodine surface treatment, 100% verification
- **Polymer Parts: End Caps, Bumper Frames and Silicone Cords**
  - Contract with Vendor, ADDIX, Includes:
    - Fabrication of Parts
    - Verification of Material Properties
- **Composite Structure**
  - Procurement of Pre-Preg Material by LLR, vendor HEXCEL
  - Contract for Cutting of Pre-Preg Plies and Preparation of Lay-ups
  - Structure Fabrication and Verification at LLR
    - Two Molds Will Be Used for Flexibility
    - The Verification Will Include:
      - Dimensional Inspection
      - Measurement of Physical Properties on Co-cured Samples
      - Structure Verification Test – Static Pull Test
  - Non Destructive Testing - Ultrasonic C-scan of the Composite Structure (Outer Walls) Is Required.

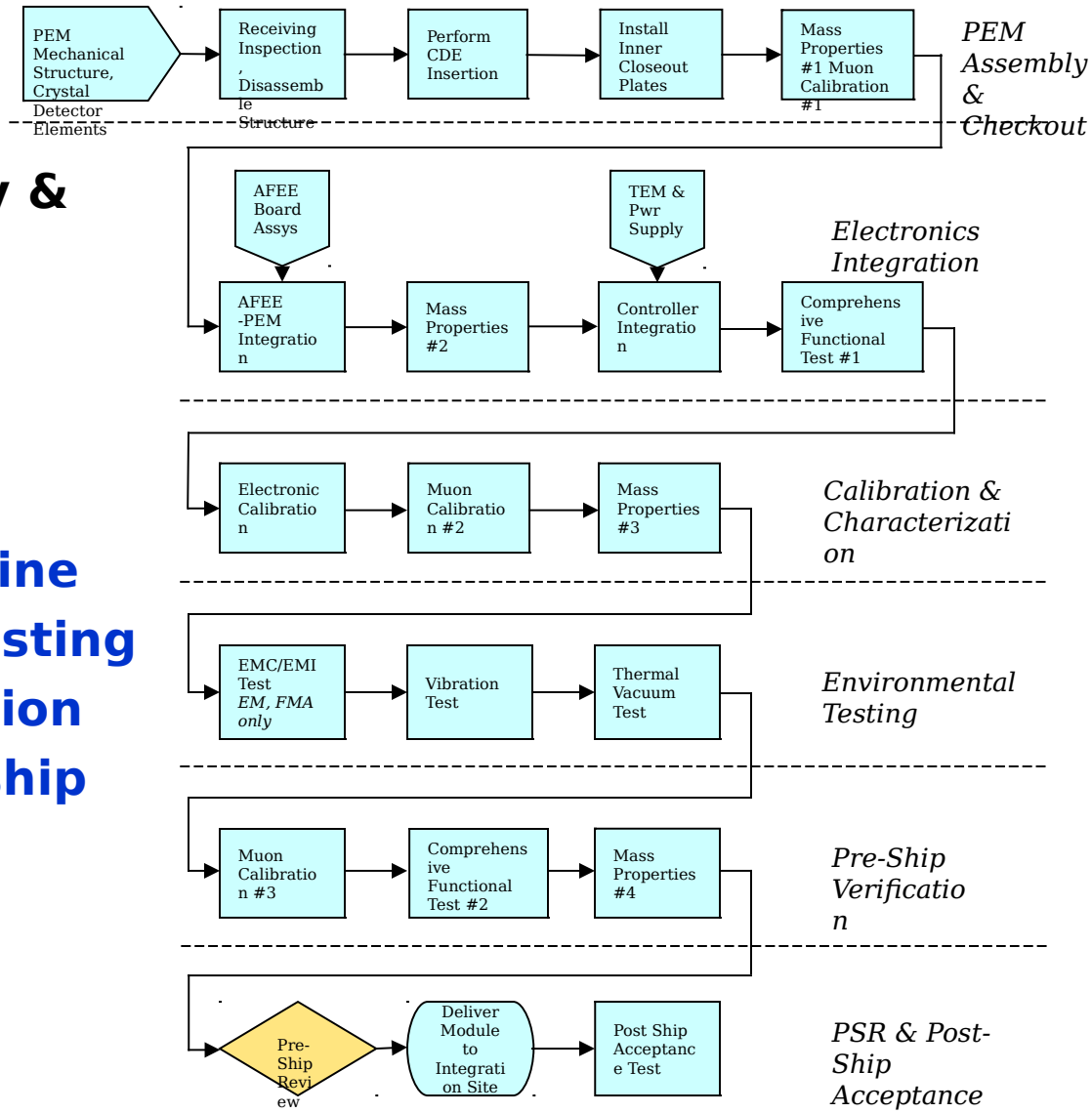
AFEE Board Fabrication

- 100 AFEE Boards to be Assembled by Qualified Vendor (need 72)
  - All Parts procured & pre-screened by NRL
  - Fabrication process monitored by in-process inspections
- AFEE Boards to undergo rigorous testing
  - Each assembly to be 100% inspected prior to test
  - Boards are thermal-cycled in groups of 12
    - Each board continuously monitored during test
    - Temp extremes of –30 and +85 deg C, w/168 hours accumulated burn-in at 85 deg C
- Testing results analyzed after each group finishes testing
  - Must yield, on average, 9 fully functional boards from each group to maintain Calorimeter Module production schedule
  - Begin rework to those assemblies with the fewest number of parts to replace
    - Use screened, burned-in parts for rework
  - Extent of rework and maximum number of parts allowed to be reworked per assy will be determined by Parts Control Board

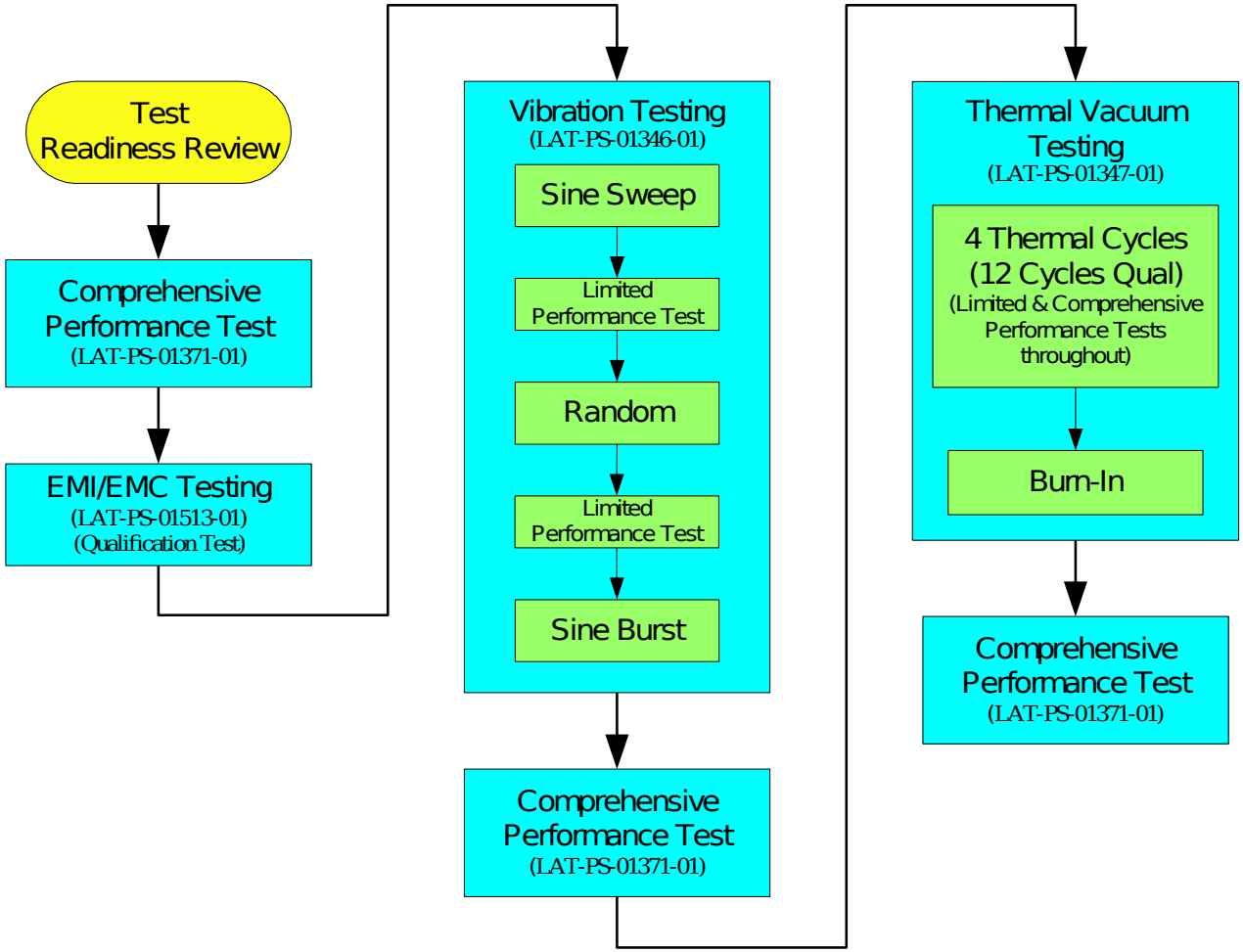
Calorimeter Module Assembly - NRL

Six Phases in Assembly & Test sequence:

1) **PEM Assembly & Checkout**
2) **Electronics integration**
3) **Calibration/Baseline**
4) **Environmental testing**
5) **Pre-ship verification**
6) **Delivery & Post-ship Acceptance**



Environmental Test Flow



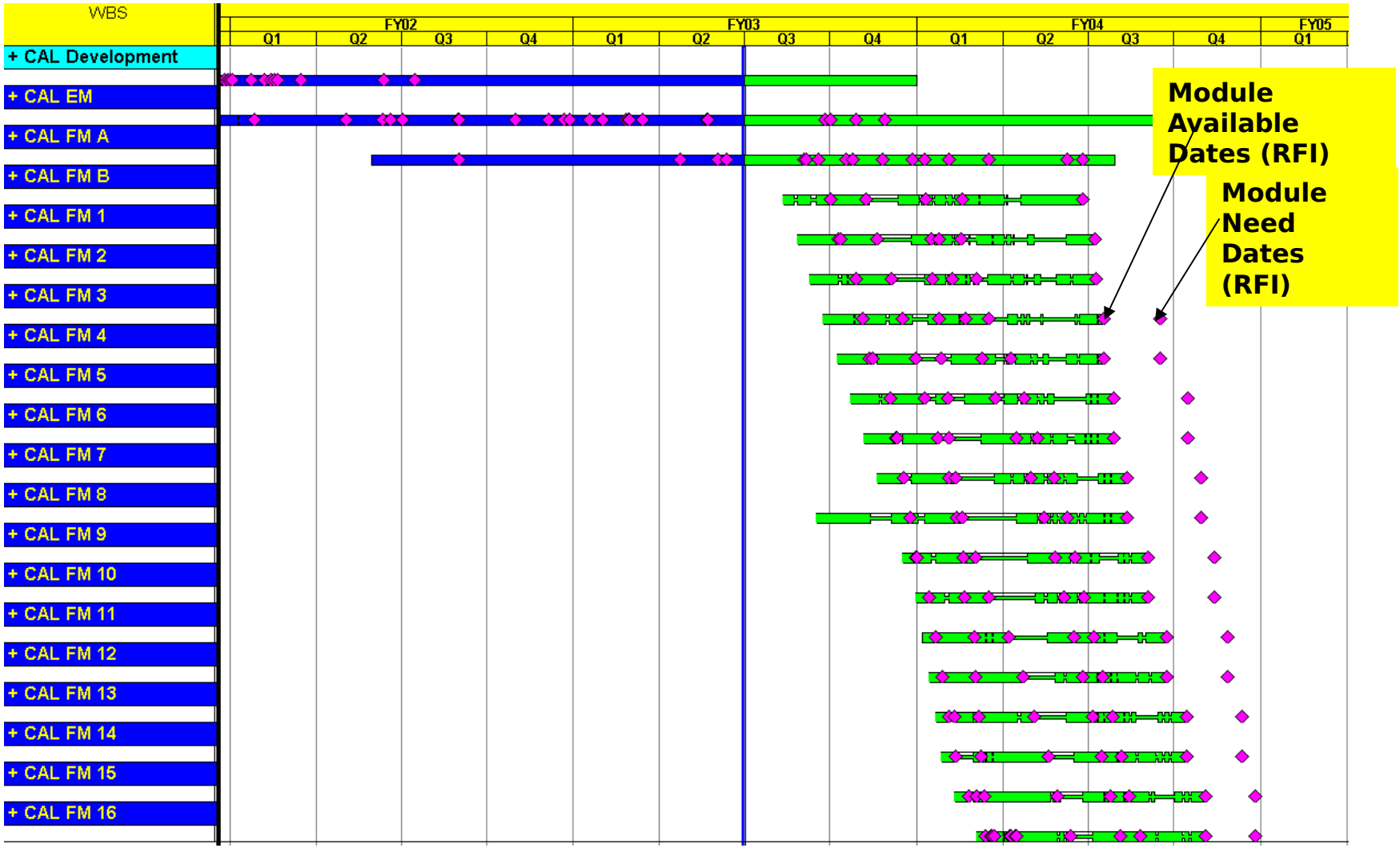
Cost and Schedule

Section 8

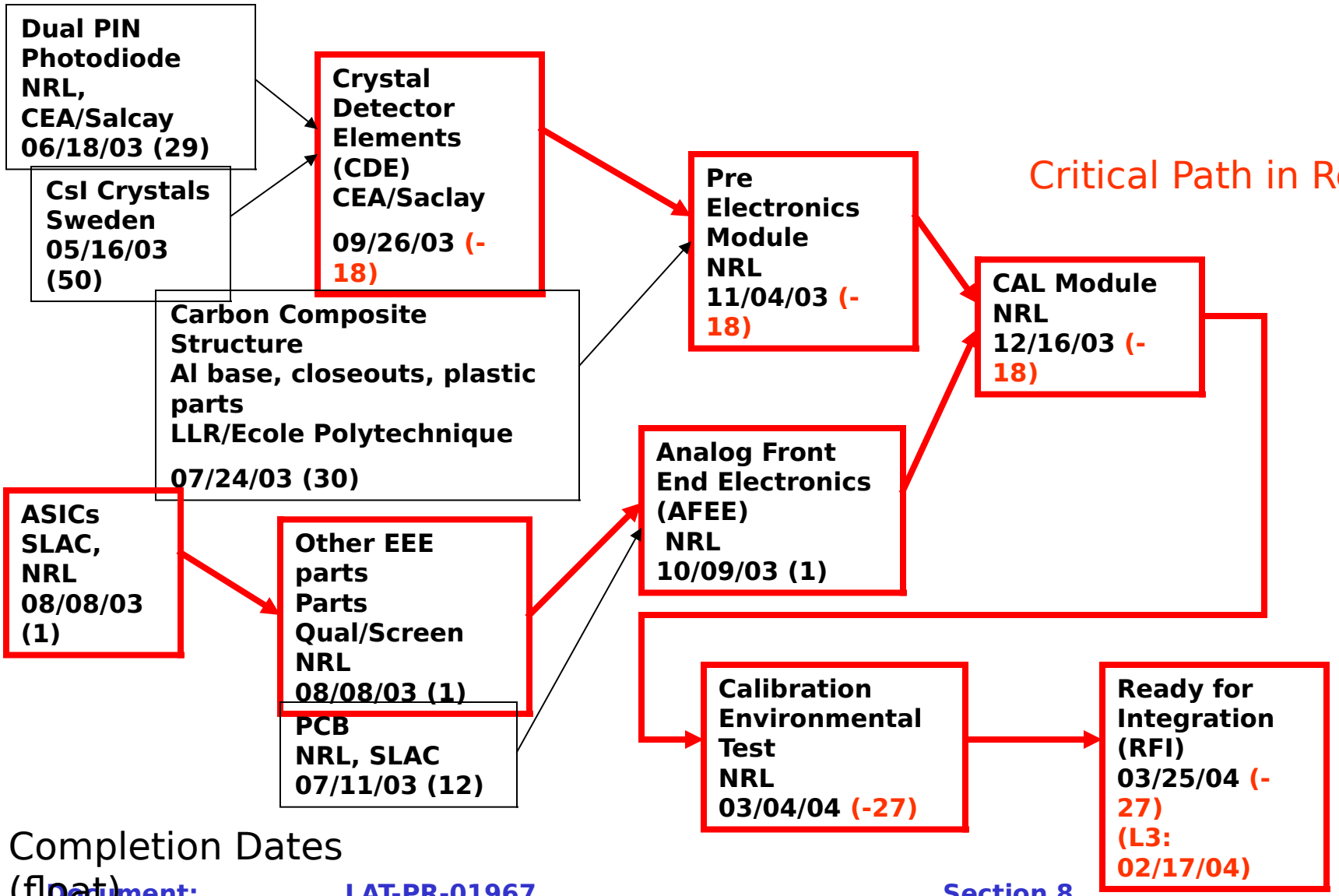
CCB Actions Affecting 4.1.5

Change Request #	Description	Status
LAT-XR-00934-01	CAL CDE Development Modifications	Approved, $227K
LAT-XR-01195-01	CAL Additional EM & FMA TV Testing	Approved, $256K
LAT-XR-01642-01	CAL Mass Allocation Reduction	Approved, -40 kg
LAT-XR-01998-01	LAT Power Allocation Update	Approved, -26 Watts

CAL Summary Schedule

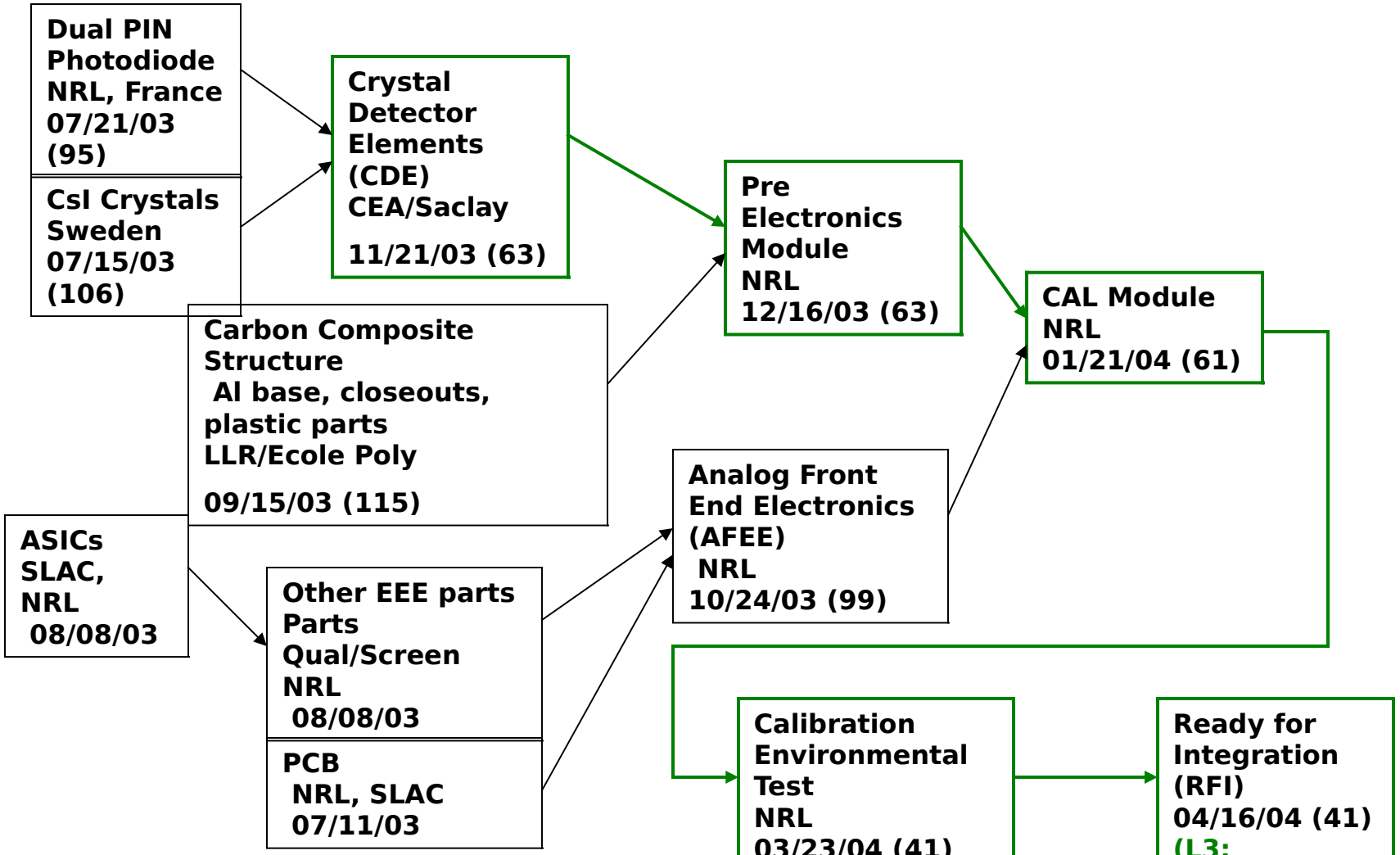


CAL Qual Module (FMA)



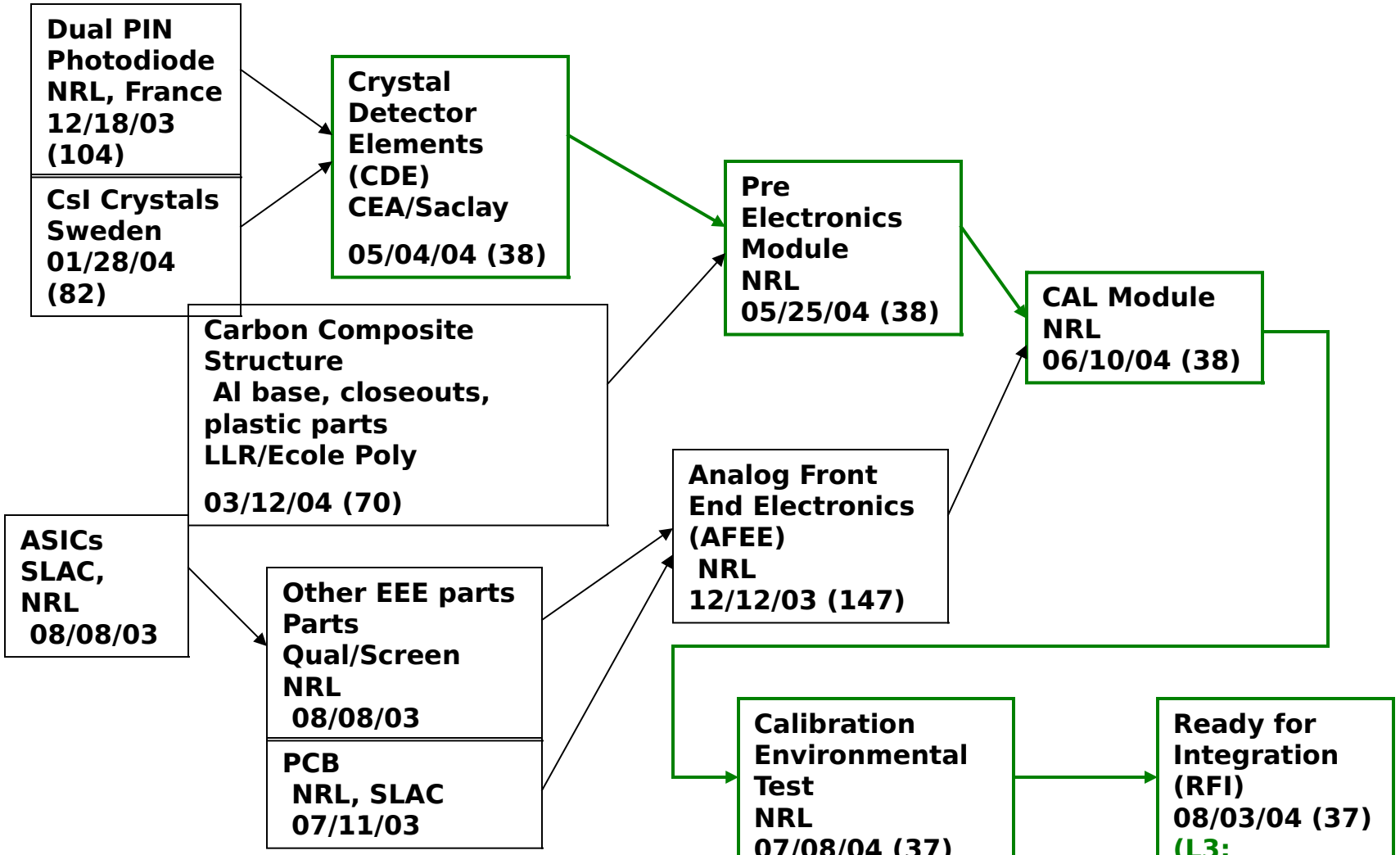
Completion Dates (float)

CAL Flight Module 3



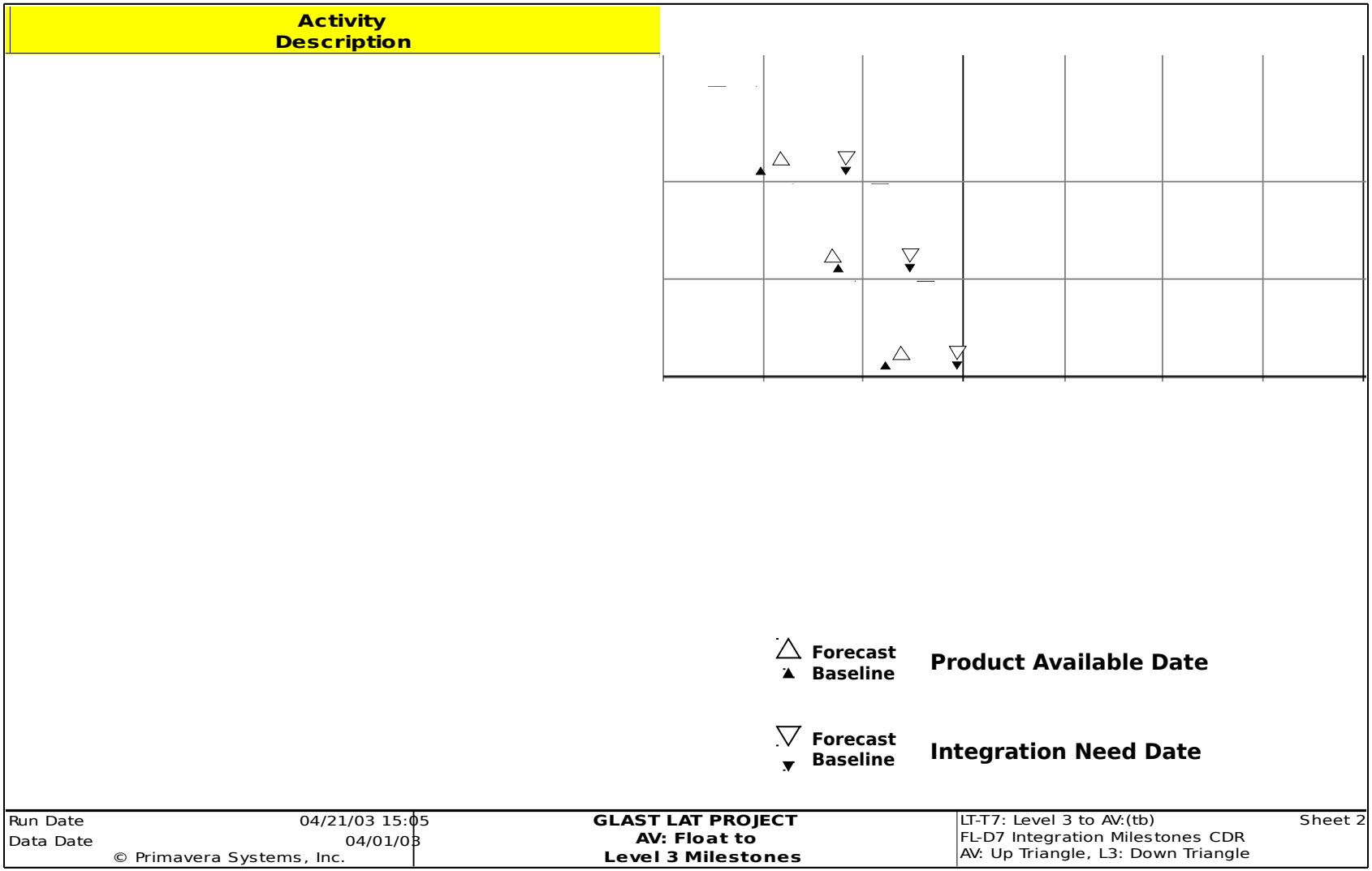
Completion Dates (float)

CAL Flight Module 16

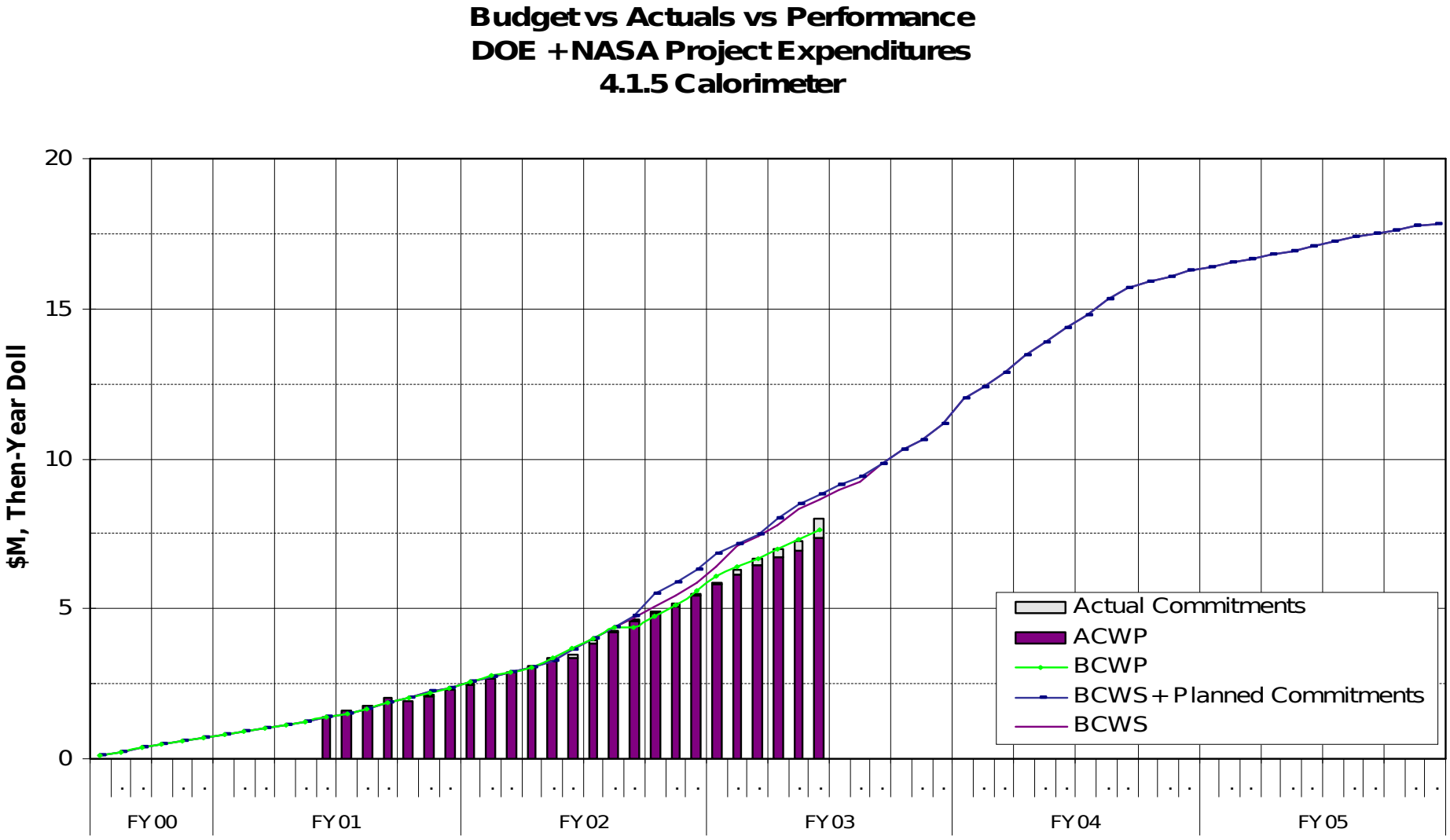


Completion Dates (float)

4.1.5 Key Deliverable Milestones



Budget, Cost, Performance



Cost/Schedule Status

- **Status as of March 31, 2003:**

Item	In k$	
Budget at Complete	17,830	
Budgeted Cost for Work Scheduled (a)	8,631	
Budgeted Cost for Work Performed (b)	7,613	
Actual Cost for Work Performed	7,372	
Cost Variance	242	3% of (b)
Schedule Variance	-1,018	-12% of (a)

CAL Procurements

Vendor	Element
Amcrys-H (Ukraine)	**CsI(Tl) crystal elements** Procurement in place by Sweden for all CAL CsI (~2000 crystals or 1640 kg) 240 prototypes in hand for Eng Model. Delivery rate: 200 crystals/month, 1st deliveries April '03
Hamamatsu Photonics	**Custom Dual PIN Photodiode** NRL and France / CEA shared procurement 600 Design prototypes in hand for Eng Model. Spec for flight version diodes completed, 184 prototypes have been procured. Flight procurement has been initiated: ~4800 diodes Delivery rate: 600 / 4 weeks. 1st deliveries June '03
3M Corporation	**VM2000 Reflective Film (CDE Optical Wrap)** Prototype in hand for EM and qualification testing. Approved for flight use.

CAL Procurements (2)

Vendor	Element
Competitive (France)	**CDE Manufacturing – bonding & wrapping** Request for proposals is out. Selection expected end of May. Delivery rate: 54 CDE/week increasing to 81 CDE/week, 1st deliveries end of Sept '03
Competitive (France)	**PIN Photodiode Assembly** Request for proposals is out. Selection expected end of May. Delivery rate: 240 PDA/two weeks, 1st deliveries Aug '03
Competitive (France)	**Mechanical Structure components** Alum. machined parts, elastomeric parts, carbon prepreg. Prototypes in hand for EM and qualification testing. Selection process complete. 1st delivery June '03

CAL Procurements (3)

Vendor	Element
MOSIS / ASAT	**ASIC manufacturing and packaging.** Prototypes in hand for EM and qualification testing. Flight ASICs have been submitted for production. Packaging procurement in process. Need date: July '03
Maxim Integrated Products	**COTS ADCs and DACs** NRL Procurement for all LAT subsystems has been completed. Qualification and screening has begun. Flight: 10,000 ADCs (MAX145), 1000 DACs (MAX5121)
QML Vendors	**EEE Parts/ Circuit Boards / Board Assembly** All parts have been approved except qualification needed for connectors and plastic encapsulated parts. All parts except Airborn connectors procured.

Risk and Summary

Section 8

CAL Risk Summary

ID #	Risk Rank	Risk Description	Risk Mitigation	Status
CAL-001	Moderate	❑ CAL ASIC performance problem. All design and manufacturing issues are not resolved. Testing with GCFE7 and GCRC4 indicate 1) continued communications problems which prevent 20 MHz communication speed at environmental margins (high temp) 2) noise performance variability as a function of pulse amplitude in some FE chips which appears related to individual FE parts but could also be PCB problem	❑ New ASICs have been submitted that should correct the communications problem. Preliminary testing of GCRC5 shows good communications to 40 MHz w/ GCFE9. More detailed testing in progress to identify margins. ❑ Noise problem has been identified and corrected in GCFE9 wafer submission. Preliminary sample testing of GCFE9 indicates problem is solved. More extensive testing in progress.	❑ On track
CAL-002	Low	❑ Failure in qualification of COTS ADC/DAC. CAL requires ~ 3500 plastic encapsulated ADCs and 300 DACs ❑ There are no options to the COTS ADC/DAC which meet LAT power and deadtime requirements	❑ Radiation testing was integral to part selection. Selected Maxim ADC and DAC were tested for radiation susceptibility over a year ago. Qualification testing is a repeat ❑ Flight DAC parts are in hand, ADCs arrive soon. A qualification program has been developed and approved by GSFC. GSFC is preparing for qualification testing.	❑ On track

CAL Risk Summary (2)

ID #	Risk Rank	Risk Description	Risk Mitigation	Status
CAL-003	Low	❑ Failure in qualification of plastic encapsulation of flight ASICs. Asics designs have not been tested to qual level so far	❑ Using earlier version of ASICs packaged by proposed flight vendor we have initiated plastic encapsulated module evaluation with GSFC. Acoustic microscopy, HAST testing has been performed ❑ Qualification program has been developed and approved by GSFC.	❑ On track
CAL-004	High	❑ Delay in deliveries of flight CDEs ❑ Our French collaborators are in the middle of a competitive procurement for the industrial partner that will fabricate all flight CDEs. The procurement process must follow French law and is potentially subject to the delay of administrative reviews ❑ The selected industrial partner must design and fabricate appropriate tooling, develop controlled manufacturing process, fabricate and qualify CDE prototypes, and then fabricate 108 CDE for the CAL Qual model by mid Sept, 2003	❑ A higher CDE manufacturing rate is an option to the French contract but may present financial and technical risks. The higher rate would deliver the later modules on schedule.	❑ Getting worse

CAL Risk Summary (3)

ID #	Risk Rank	Risk Description	Risk Mitigation	Status
CAL-005	Moderate	❑ CAL module subsystem performance problem detected in EM module test program ❑ The CAL EM is the first opportunity for subsystem level testing of module performance. Issues such as noise, cross talk and correlation of measurements at two ends of CDE will be examined in detail for the first time	❑ Testing at the AFEE board level with prototype boards and earlier version of ASICs give some confidence. However, problems were identified that could be related to PCB board layout or ASIC design problems ❑ Accelerator beam testing of the assembled calorimeter is the best confidence test for the calorimeter electronic design. The schedule puts the calorimeter beam test after flight circuits have begun fabrication. Mitigation for electronic problems determined at beam tests is severe	❑ On track
CAL-008	Low	❑ CAL AFEE board design, SMT manufacturing, testing, PEM assembly and qualification issues still to be resolved, since these processes have not been validated so far	❑ Remaining EM boards have been fabricated using SMT processes and we will analyze any issue related to design, layout and manufacturing. ❑ Prior to start of flight manufacturing, assembly processes and procedure will again be validated	❑ On track

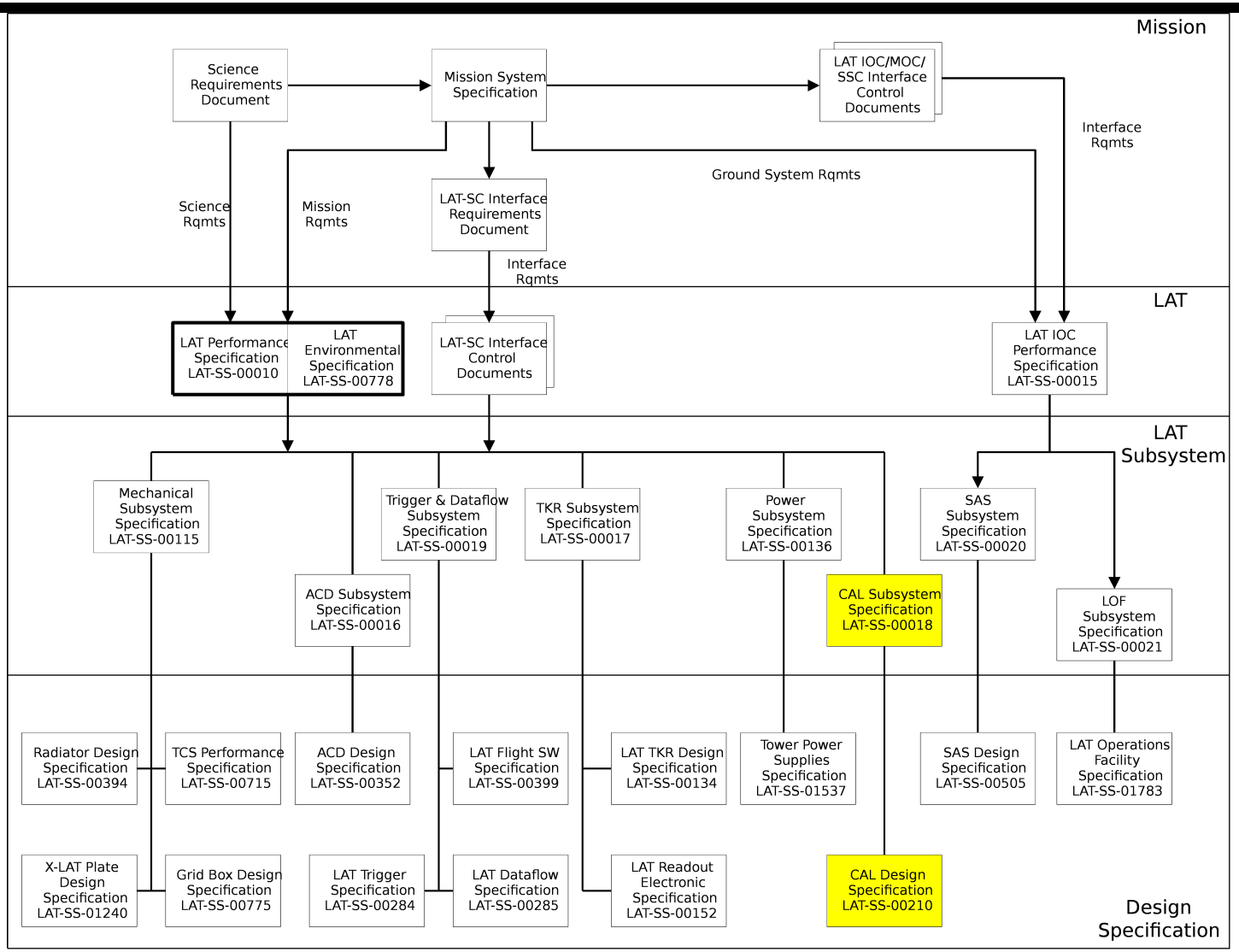
Summary

- The technical design of the CAL module is mature and verified
  - Most outstanding issues will be retired at the completion of EM test program in June
  - New PIN photodiode verification will complete as well in June
  - Updated ASIC versions will be verified in May
  - Essentially all documents are released
- The CAL schedule is aggressive in meeting almost all Level 3 milestones with appropriate schedule contingency
  - Recently discovered problem in deliveries of CDE make delivery of 1st four modules late by ~ 1 month.
  - Additional compression of the manufacturing schedule succeeds in preserving approx. baseline deliveries on later modules.
- CAL is ready for flight production
  - Technical risks are minimal
  - CAL schedule has been compressed to the limit

Appendix A. Requirements

Section 8

Requirements Flow



CAL Level III Requirements

Reference: LAT-SS-00018

Parameter	Requirement	Verification	Expected Performance
Energy Range	20 MeV – 300 GeV 20 MeV – 1 TeV (goal) 5 MeV – 100 GeV, single crystal	Simulation, Beam Tests	Required performance ~2 MeV threshold (BOM)
Energy Resolution (1 sigma)	< 20% (20 MeV < E < 100 MeV) < 10% (100 MeV < E < 10 GeV) < 6% (10 GeV < E < 300 GeV, incidence angle > 60 deg)	Simulations and EM and LAT calib unit Beam Tests	Simulations demonstrate required performance
Energy Resolution (1 sig) Single Crystal	< 2% for Carbon Ions of energy >100 MeV/nuc at a point.	EM (and Calib Unit) beam test	< 0.5% (correlation of ends removes Landau)
Design	Modular, hodoscopic, CsI > 8.4 RL of CsI on axis	Inspection	8.6 RL
Active Area	>1050 cm^2 per module < 16% of total mass is passive mtrl.	Inspection	1080 cm^2 per module < 14% is passive
Position Resolution	< 3 cm in 3 dims, min ionizing particles, incident angle < 45 deg.	Test with cosmic muons, all modules	< 1.5 cm in longitudinal measurement
Angular Resolution	15 $\times \cos(\theta)$ deg, for cosmic muons in 8 layers	Test with cosmic muons, all modules	8 $\times \cos(\theta)$ deg
Dead Time	< 100 μs per event < 20 μs per event (goal)	Test	< 19 μs per event

CAL Level III Requirements (cont)

Parameter	Requirement	Verification	Expected Performance
Low Energy Trigger	>90% efficiency for 1 GeV photons traversing 6 RL of CsI <2 μs trigger latency	Simulations	>93% <1 μs
High Energy Trigger	>90% efficiency for 20 GeV photons depositing at least 10 GeV <2 μs trigger latency	Simulations, Calib unit test in beams	>91% <1 μs
Size (module)	<364 mm in width (stay clear) <224.3 mm in height (stay clear)	Inspection	363 mm 224 mm
Mass	<1440 kg (90.0 kg/module)	Test	1376 kg
Power	<65 Watts (conditioned) (4.05 W/module)	Test	<54 Watts (conditioned)
Temperature Range	– 10 to +25 C, operational – 20 to +40 C, storage – 30 to +50 C, qualification	Subsystem TV Test 4 cycles, acceptance 12 cycles, qualification	Required performance
Reliability	>96% in five years	Analysis	>98% in five years (15/16 modules) LAT-TD-00464-03

Derived Requirements

- LAT CAL Subsystem Level IV Specification – LAT-SS-00210
  - Contains 164 detailed design requirements derived from CAL Level III Specification – LAT-SS-00018
- LAT CAL Verification & Environmental Test Plan – LAT-SS-01345
  - Details approach to verifying each Level IV requirement
    - Lists verification methods used
      - Mostly verified by Test, 53 reqmts verified by analysis/inspection
    - Assembly levels at which verification is performed
      - 114 requirements are verified at the components level

Level IV (Derived) Requirements

Document Title	Document Number	Status
LAT-CAL Subsystem Level IV Specification	LAT-SS-00210-03	Released
CAL-LAT Interface Control Document	LAT-SS-00238-04	Released
CAL-LAT Interface Definition Drawing	LAT-DS-00233-03	Released
CAL Module Verification & Environmental Test Plan	LAT-SS-01345-01	Released
CAL Module Assembly, Test, and Calibration Requirements	LAT-SS-00222-01	Released
CAL Performance Acceptance Standards & Tests	LAT-SS-00231-01	Released
CAL Module Assembly & Test Plan	LAT-MD-00262-02	Released
CAL Mechanical Structure Specification	LAT-SS-00241-03	Released
CAL Flight CsI Crystal Detector Element Specification	LAT-SS-01133-02	Released
CAL CsI Crystal Performance Specification	LAT-SS-00820-03	Released
CAL Flight Dual PIN Photodiode Specification	LAT-DS-00209-12	Released
CAL Analog Front End Electronics Board Specification	LAT-SS-00278-02	Released

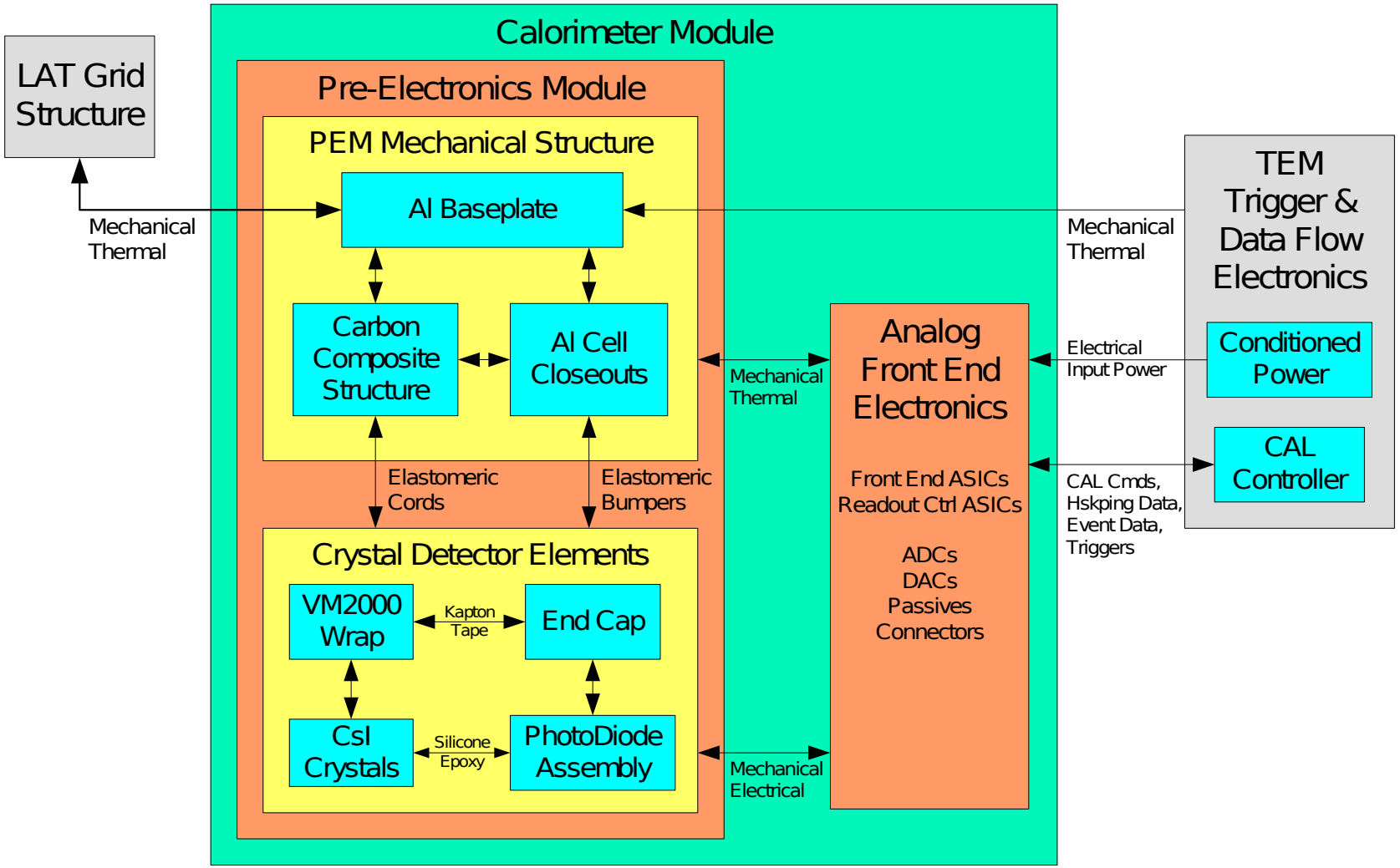
Level IV Requirements Compliance

Parameter	Requirement	Verification	Expected Performance
Low Energy - Input PIN Diode - Noise	2 MeV – 1.6 GeV 5000 e^-/MeV < 2000 e^-	Analysis, Test	Compliance
High Energy - Input PIN Diode - Noise	100 MeV – 100 GeV 800 e^-/MeV < 2000 e^-	Analysis, Test	Compliance
Overload Recovery	< 100 μs for x1000 overload	Analysis, Test	Compliance
Absolute Light Yield	>7000 electrons per MeV for the large diode >1100 electrons per MeV for the small diode	Test	Compliance
End to End Light Yield Ratio	The ration of the light yields of the large diodes on either end of the CDE shall be between 0.90 and 1.11	Test	Compliance
Small to Large Diode Light Yield Ratio	The ratio of the light yields between the large and small diodes of each Dual PIN Photodiode shall be between 5 and 7	Test	Compliance
Muon Energy Resolution	The width of the distribution of measured energies from sea-level muons (energy resolution, 1 sigma) shall be <8%	Test	Compliance
Light Tapering	The light yield at 2 ± 1 cm from the opposite crystal face shall be 60% ± 10% of the light yield at 2 ± 1 cm from the crystal face to which the large diode is bonded	Test	Compliance
Radiation Susceptibility	Insensitive to LETs > 37 MeV/(mg/cm^2) (SEU) Shall meet performance req after total radiation dos of 10 kRad (TID) No latchup at LETs < 60 MeV/(mg/cm^2) (SEL)	Analysis, Test	Will tolerate specified radiation environment with no performance degradation over design lifetime (5 years)
Physical Interfaces & Clearance			
- Dimensions & Tolerances	LAT-DS-00233 (CAL IDD) LAT-SS-01133 (CDE Spec)	Inspection	Compliance
- Surface Condition of Tabs	LAT-DS-00233 (CAL IDD)	Inspection	Compliance
- Static Stay-Clear Dimensions	LAT-DS-00233 (CAL IDD)	Inspection	Compliance
- Dynamic Stay-Clear Dimensions (per LAT-SS-00238)			
- Lateral	0.50 mm MAX	Inspection	Verified on VM2, < 0.3 mm
- Vertical	0.50 mm MAX	Inspection	Verified on VM2, < 0.3 mm

Level IV Requirements Compliance (cont)

Parameter	Requirement	Verification	Expected Performance
Base Plate Requirements	(per LAT-SS-00238)		
- Stiffness	Equivalent to 8 mm Al Plate	Analysis	Equivalent to 8 mm Thickness (Plus Margin)
- CTE	CTE = 21-25E-6 m/m/deg C	Analysis	Aluminum Plate
Mass Properties	(per LAT-SS-00238)		
- Center of Gravity	Max Lateral Offset +/-10 mm	Analysis	Shows within +/- 1 mm
	Max Z CG Position = 116 mm	Analysis	Zcg = 87.5 mm from CAL-Grid Interface
Structural Load Environment	(per LAT-SS-00238/LAT-SS-00778)		
- Static-Equiv. Accelerations	Lateral = +/-6.0 g Axial = +6.8/-1.8 g	Analysis, Test	Verified on VM2. To be Re-verified on EM (Analysis Shows Positive Margins)
- Random Vibration	LAT-SS-00778	Analysis, Test	Verified on VM2. To be Re-verified on EM (Analysis Shows Positive Margins)
- Interface Limit Loads	4373 N max across tab	Analysis, Test	To be Verified on EM (Analysis Shows Positive Margin)
- Interface Distortion Limit Loads	0.25 mm max distortion	Analysis	Analysis Shows Positive Margin
- TEM Interface Loads	Tension = 3750 N Compression = 2625 N Shear = 1288 N Bending Moment = 19.3 Nm	Analysis, Test	To be Verified on EM (Analysis Shows Positive Margin)
Thermal Environment	(per LAT-SS-00238/LAT-SS-00778)		
- CAL-Grid Conductance	>0.03 W/cm^2 deg C	Analysis	Analysis uses 0.25 W/cm2 deg C Analysis to be updated following EM Testing
- CAL-TEM Contact Conductance	0.1 W/deg C	Analysis	Analysis used 0.1 W/deg C Analysis to be updated following EM Testing
First Natural Frequency	> 50 Hz	Analysis, Test	Verified on VM2 and by Analysis (>150 Hz) To be Re-verified on EM
Venting	per LAT-SS-00238/ LAT-SS-00778	Analysis	Analysis Shows Positive Margin
Preserve Safety of CDEs	No Light Yield Change	Analysis	Verified on VM2
Contamination/Particulates	per LAT-SS-00238	Analysis	All Particulates Generated from Fracture-Sensitive Materials will be Contained within the Stay-Clear Volume of the CAL
	per LAT-MD-00404	Analysis	All materials approved for flight Structural cleanliness addressed during assembly Bake out of all composite and polymer materials

Calorimeter Interfaces



Mass Budget

The Calorimeter Subsystem meets LAT rqmts with a margin of 4.6%

Component	Material	Mass (kg)
Crystal Detector Elements	CsI Crystals	74.24
	Diodes, wire, wrapping	0.800
Composite structure	Graphite epoxy	2.874
Structure shell	Aluminum	5.783
Dampers	Silicone	0.230
AFEE Circuit Card Assy's (incl AFEE – TEM cables)		1.660
Fasteners, miscellaneous		0.400
CAL Module Total Mass		**85.99**
Calorimeter Total Mass		**1376**
CAL Module Allocation		**1440**
Mass Margin		**64**

The total amount of passive material (non-CDE) contained in the Calorimeter (13.7%) meets LAT rqmt of < 16% (Level III – 5.5.4)

Power Budget

The Calorimeter Subsystem has a 18% power margin

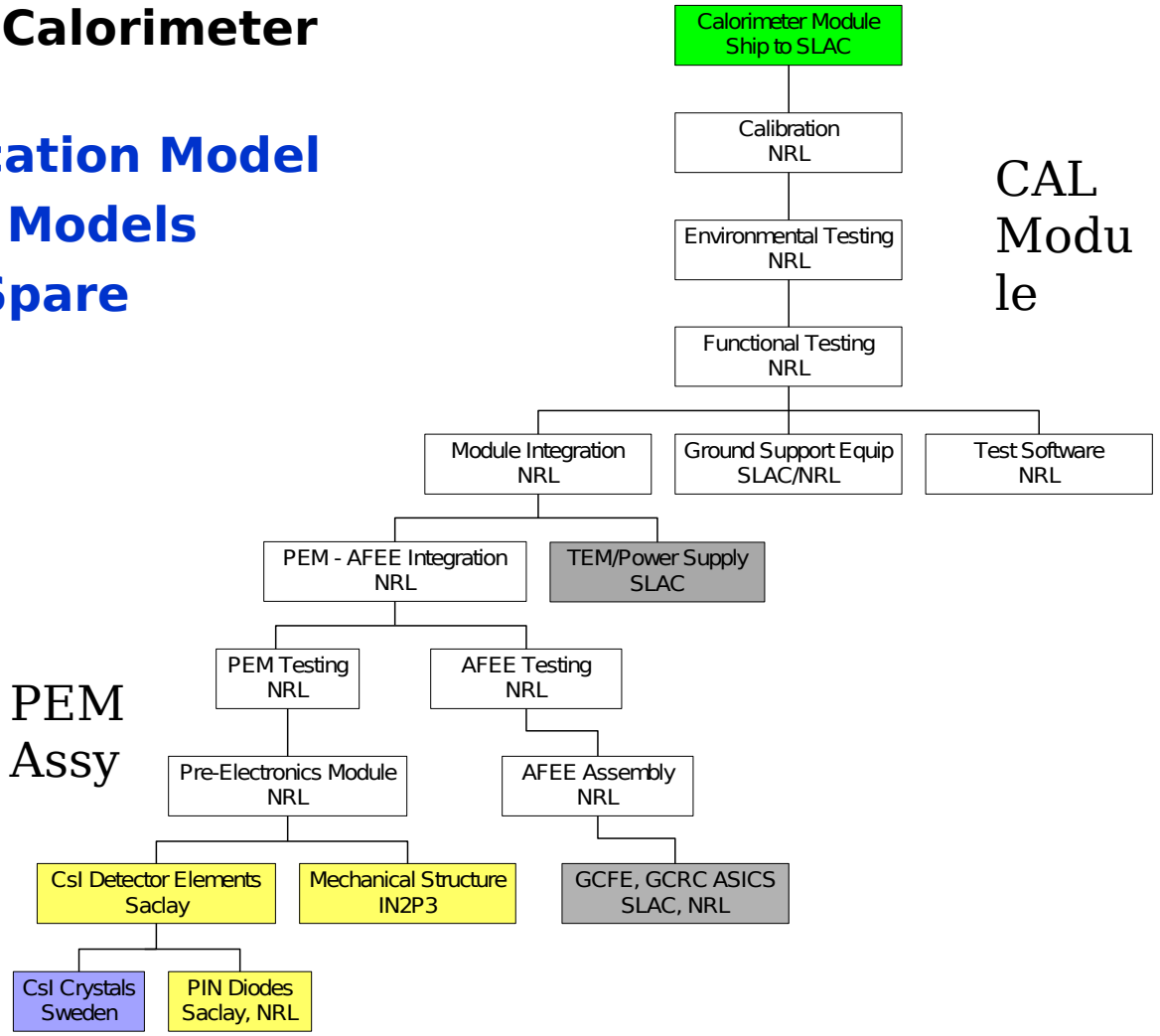
Component	Quantity	Power (mW)	
		Each	Total
GCFE	48	11.4	547
GCRC	4	64	256
ADC MAX145	48	0.042	2
DAC MAX5121	1	4.5	4.5
References	2	13.5	27
Total Power per AFEE (mW)			**836.5**
CAL Module Total Power (W)			**3.35**
Calorimeter Total Power (W)			**53.5**
Calorimeter Allocation (W)			**65.0**
Power Margin (W)			**9.5**

Appendix B. Fabrication Process

Section 8

Calorimeter Assembly Overview

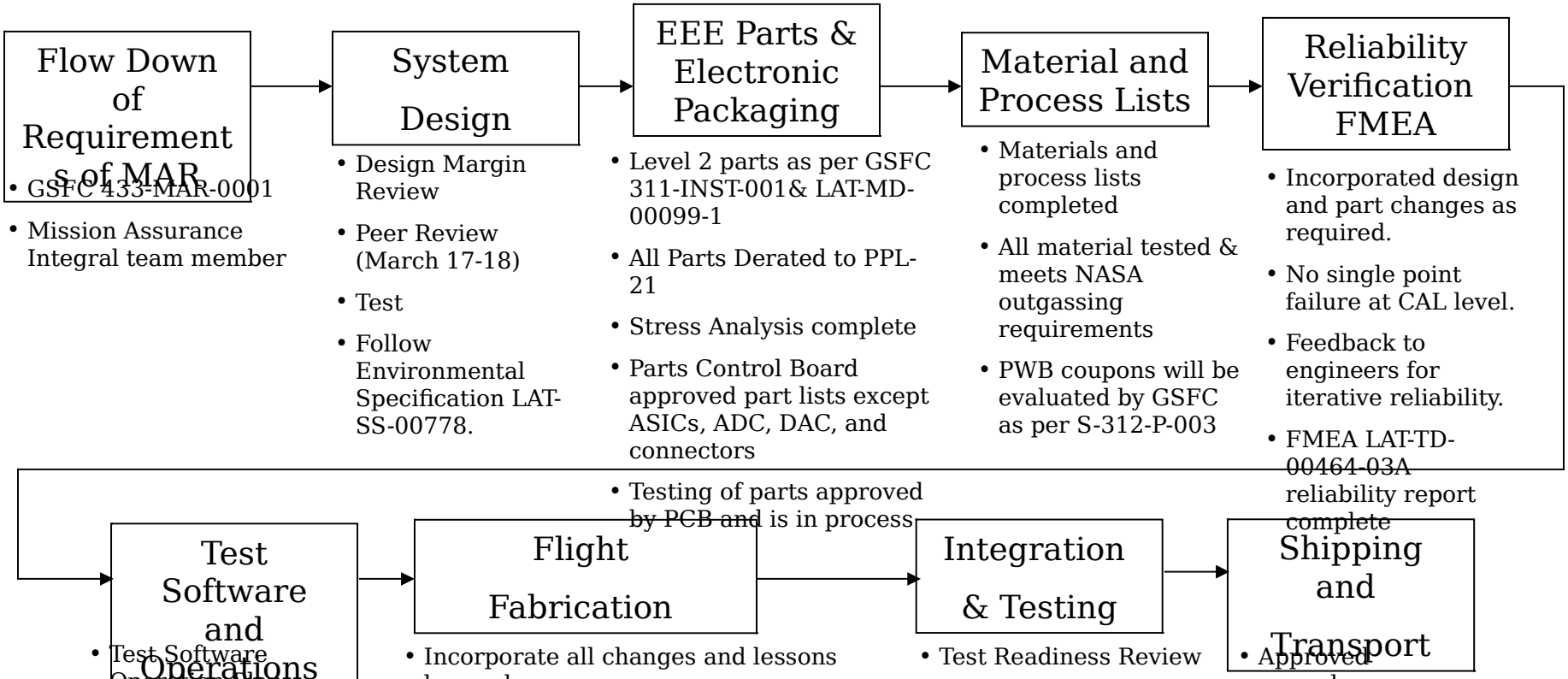
- **18 Identical Calorimeter Modules**
  - **1 Qualification Model**
  - **16 Flight Models**
  - **1 Flight Spare**



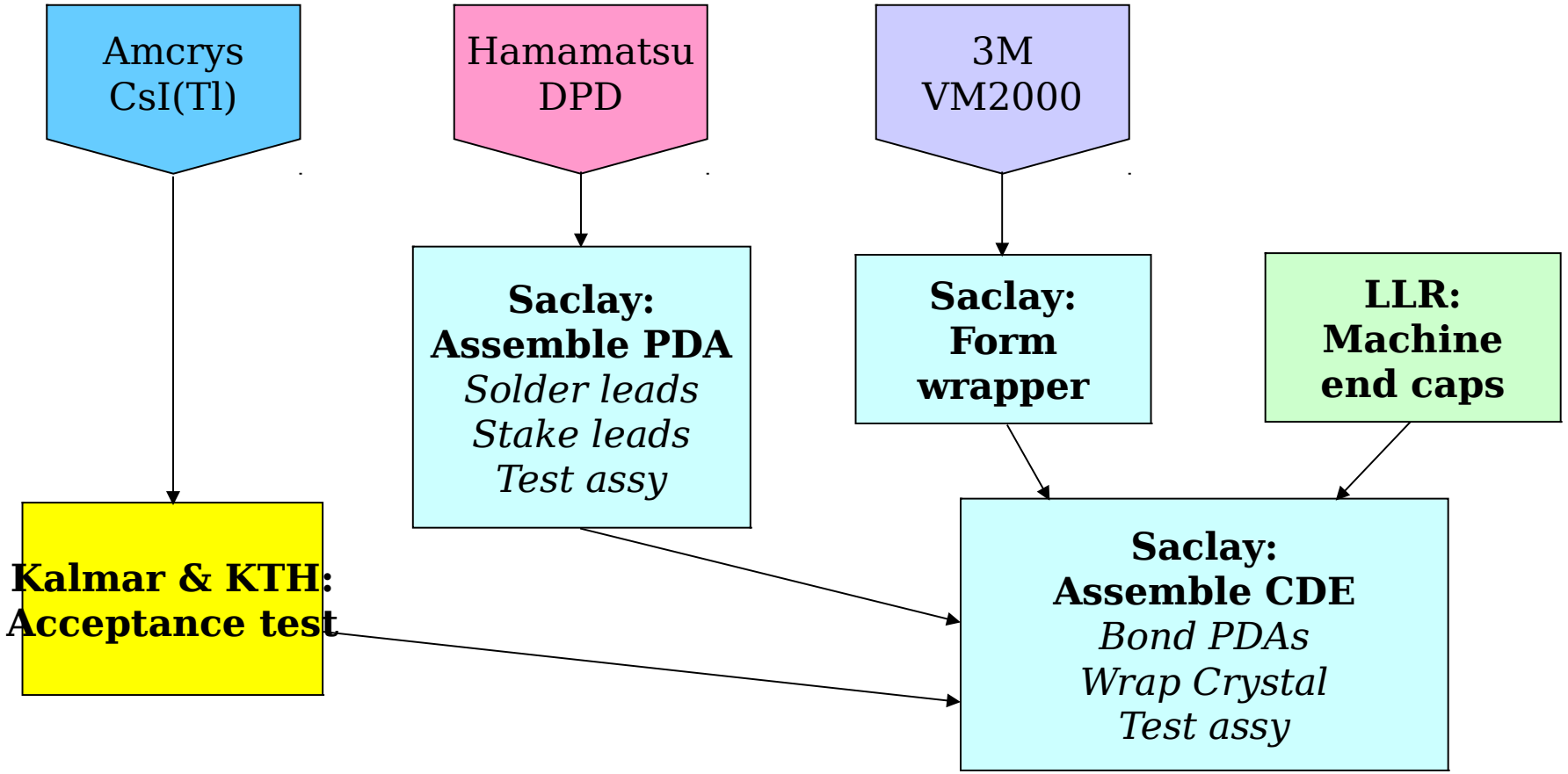
Manufacturing and Reliability

- Manufacturing, process control and assembly methods, procedures and tools have been defined and are being implemented in order to mitigate risks related to processes and workmanship issues.
- For each configuration item at NRL, CEA, IN2P3, and other subcontractors, defined and controlled procedures were implemented during Engineering Model (EM) design, fabrication, and testing for the mission requirements.
  - All work was performed using closed loop work order authorization and all non-conformances were recorded.
  - These procedures will be modified from the lessons learned prior to flight fabrication and testing.
- This will ensure that the design, fabrication, in-process control and testing procedures and processes guarantee that the design is producible and verifiable.
- Before fabrication of flight hardware several peer reviews, manufacturing readiness reviews, and test readiness reviews will be conducted.

Manufacturing and Reliability



CDE Manufacturing Responsibilities



- Assembly flow for CDEs

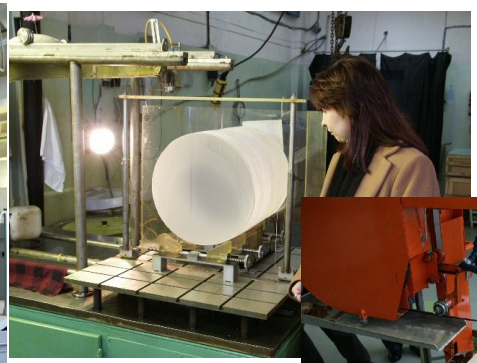
Crystal Procurement Status

- Contract and procurement process by Swedish Consortium
  - Competitive selection of vendor began Dec 2000
  - Final selection of Amcrys-H in Feb 2001
    - Final contract crystal spec (LAT-DS-00095-05) completed after negotiation with vendor
  - Prototype crystals delivered May 2001 – Apr 2002
    - 244 EM xtals manufactured to LAT-DC-00095-05
  - Xtal dimensions (for EM and FM) modified Feb 2002
    - From review of tolerances of CAL components and build-up of tolerances
      - Xtals shortened by 7 mm (333 mm became 326 mm)
      - Chamfers enlarged and better defined
  - Revised specification Feb 2002
    - CAL CsI Crystal Performance Specification LAT-DS-00820-03
      - All EM xtals remachined at Amcrys and Kalmar to comply with new dimensions, Jun-Oct 2002
  - 48 prototype xtals built to new spec arrived Kalmar Feb 2003
- Successful flight Procurement Readiness Review Feb 2003
  - First flight xtal delivery to Kalmar expected Apr 2003
  - Total flight purchase: 1945 xtals

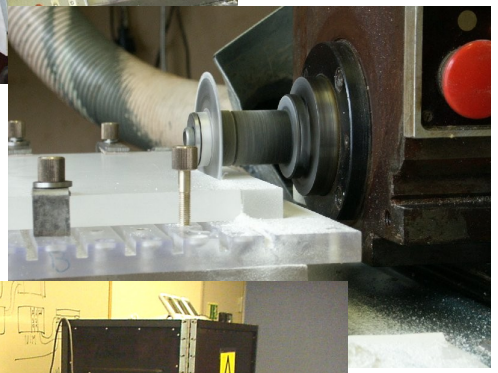
Crystal Production Flow (Ukraine and Sweden)

Boule growing - Making boule samples - (Rad testing in Sweden) - Machining crystal logs - Polish crystal - Verify mechanical dimensions, marking - Resting - Light tuning - Tyvek and alum-foil wrapping - Vacuum-packing - Shipping to Sweden (Kalmar) - Checking documents and storage - Mechanical and optical acceptance test - Vacuum-pack in CEA V-block - Distributing results (CEA, NRL) - Packing in CEA-container - Shipping to CEA via Gondrand

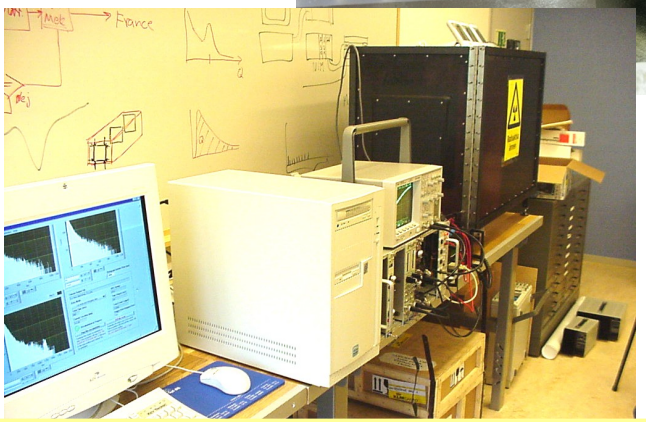
Crystal Production Flow



Crystal Cutting



Crystal Growing



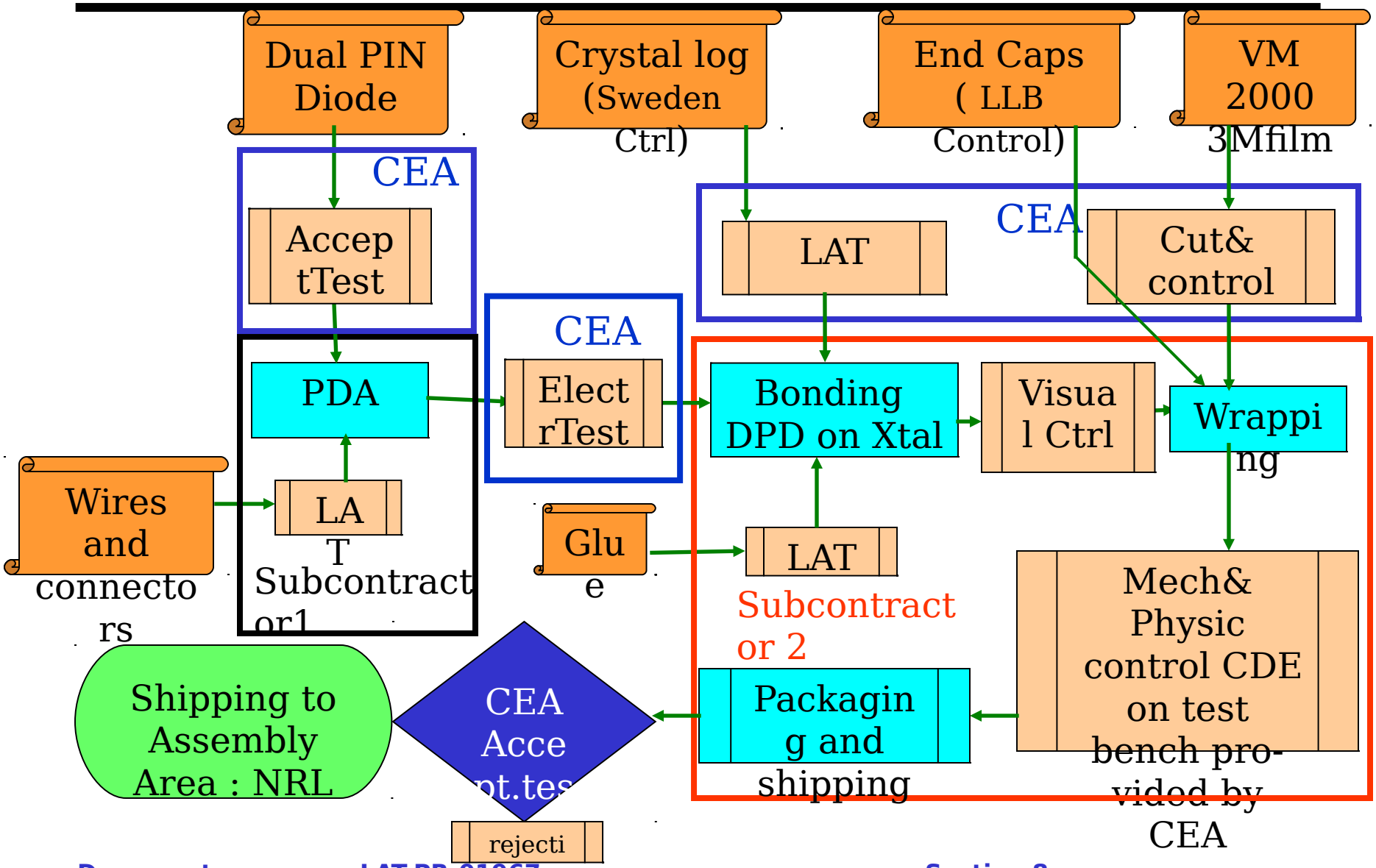
Crystal Polishing

Crystal Mechanical and Optical Acceptance Testing

CEA Program Status

- LoA between NASA and CNES
  - final draft approved by both parties, awaiting resolution of funding
- MoA between SLAC, NRL, CEA:
  - signed in Jan'03
- Financial agreement between CNES and CEA:
  - budget & manpower profiles approved in Nov'02
  - new CNES financial situation: participation to GLAST recommended to the President, but cost-capped
- 14 EM-CDEs delivered to NRL in Dec'03
  - they meet the specifications & performance
  - bonding on DPD (epoxy window) & tooling design demonstrated
  - packing concept evaluated
  - Supported DPD evaluation and change to silicone optical window
- Present activities
  - evaluation of the new DPD, new PDA and new PDA bonding
  - Placing contracts for the FM PDA, CDE, GSE, & various containers

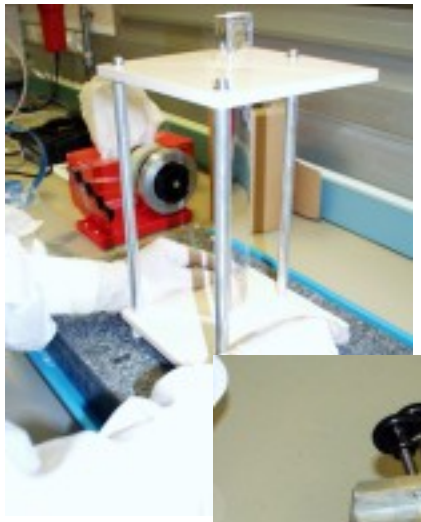
Manufacturing Plan



PDA Manufacturing Plan

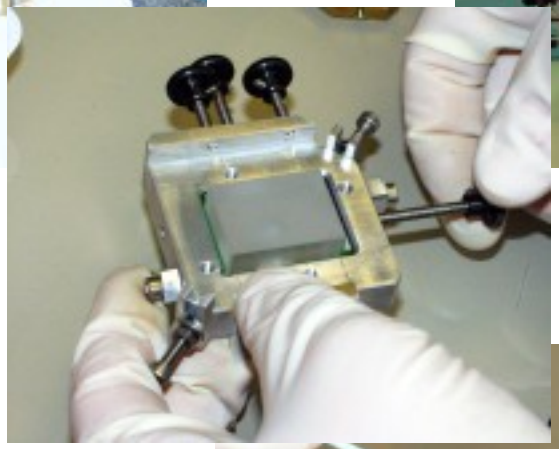
- Because of the short schedule: wire procurement before contract (> 8 weeks to manufacture)
- Contract Order: foreseen May 21
  - Call for tender : done (6 companies interested)
  - Sending specifications to selected companies (mid March)
  - Answers from the companies: (end April)
  - Opening letters and ask for additional information
  - Write & sign the contract and place the order
- Preparation &training (molding tools, encapsulant product…)
  7 weeks
- Manufacturing lot 1 of 264 PDA (begin. July to begin. Aug)
- Manufacturing lot 2 of 240 PDA (in August)
- Manufacturing lots 3 to 20 (240 PDA /2 weeks)

PDA-Crystal Bonding Process Overview

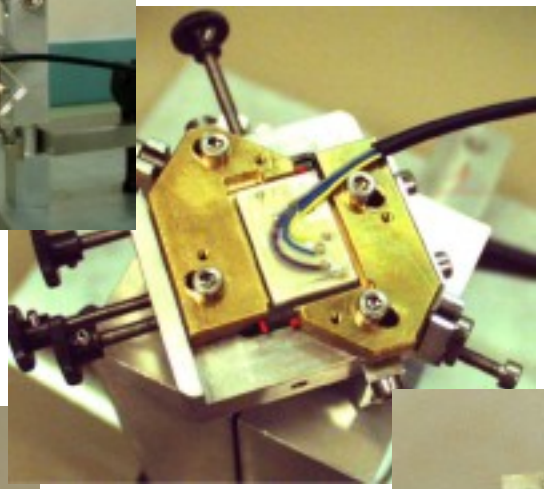


End face polishing

Mold tooling & Glue injection



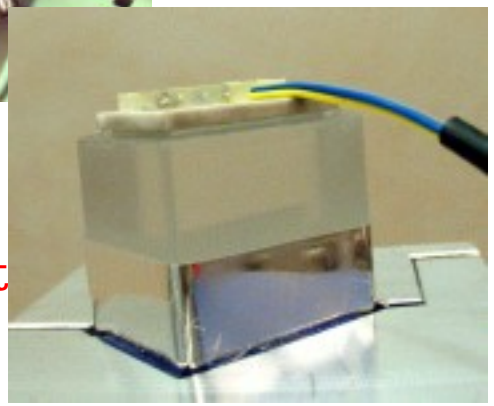
Support tooling



Mold removal after 24 hours

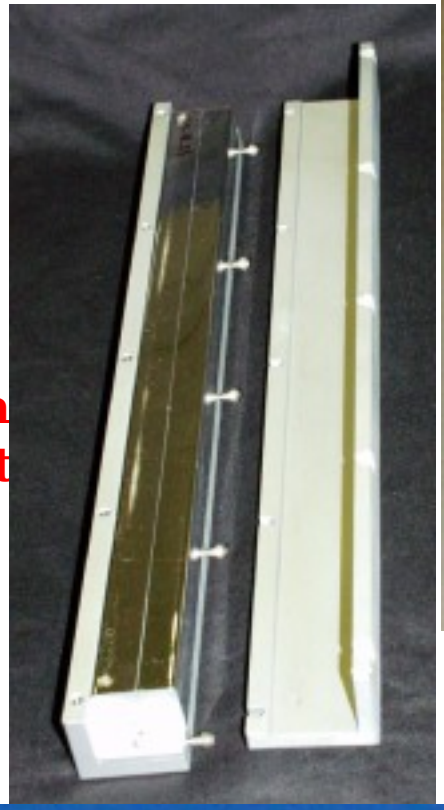
Primer deposition

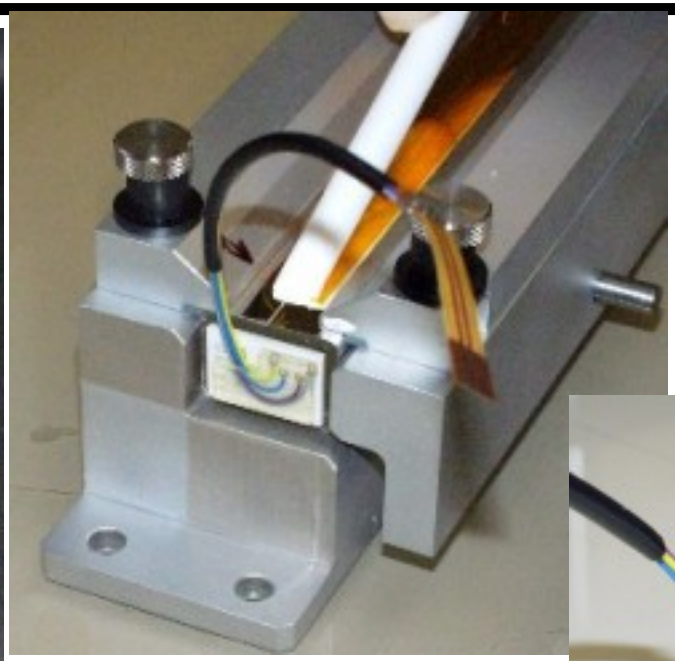
Polymerization time = 7 days



Wrapping overview

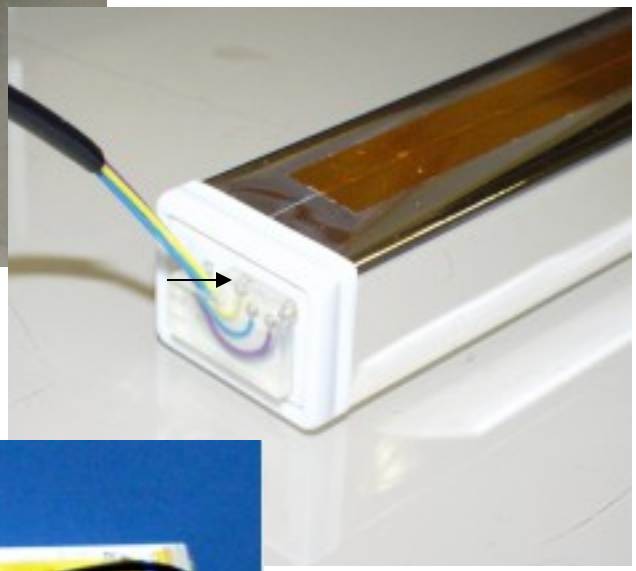
VM2000 foil shaped around a kernel at 120°C

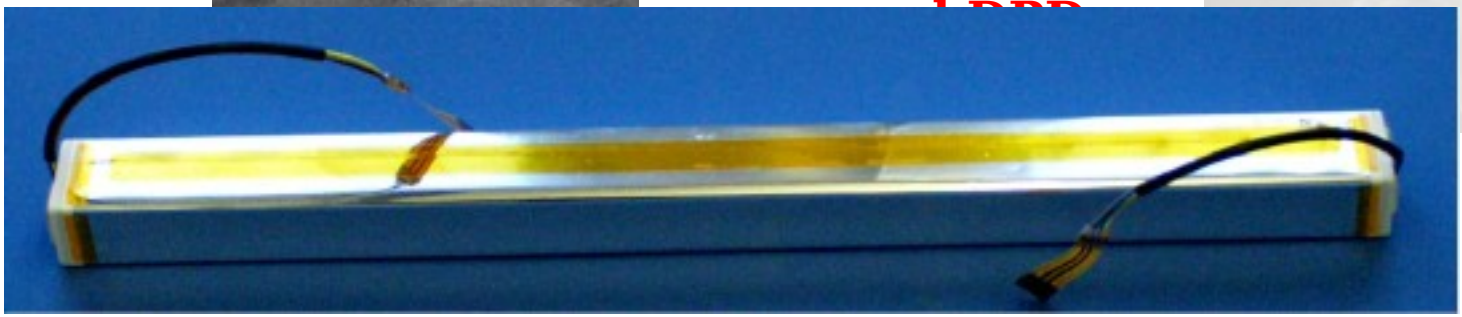




VM2000 foil wrapped and pasted

Mounting of the end cap

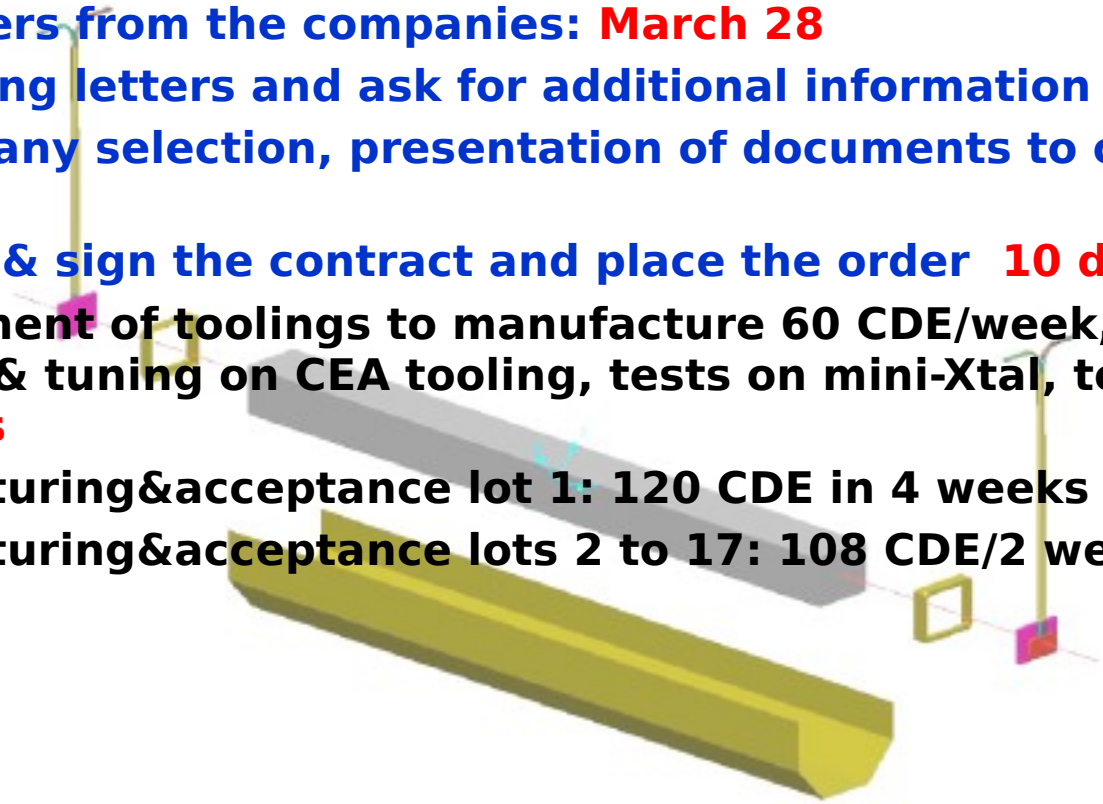




Wrapped CDE

CDE Manufacturing Plan

- Same manufacturer does bonding & wrapping
- Order foreseen May 26
  - Call for tender : done (6 companies interested)
  - Sending specifications to selected companies: done Feb. 13
  - Answers from the companies: March 28
  - Opening letters and ask for additional information < 2 weeks
  - Company selection, presentation of documents to committee: 20 May
  - Write & sign the contract and place the order 10 days
- Procurement of toolings to manufacture 60 CDE/week, process practice & tuning on CEA tooling, tests on mini-Xtal, tests of 12 CDE: 3 months
- Manufacturing&acceptance lot 1: 120 CDE in 4 weeks in Sept
- Manufacturing&acceptance lots 2 to 17: 108 CDE/2 weeks Mid May '04



CDE System/Verification plan

- **EVALUATION: characteristics and margin studies**
  - **DPD S8576-01 (Silicone window, Lead tinning):**
    - 11 S8576 with Silicone encapsulant
    - 184 S8576-01 (DPD pre-FM-series)
  - **PDA (solder, staking, wires):** DPD pre-series
  - **Bonding (tooling, process):** DPD pre-series + mini Xtal
- **QUALIFICATION: Specification requirements**
  - **DPD S8576-01**
    - **Tinned ceramic:** 1% by lot
    - **Die:** 5 by wafer lot
    - **Assembly:** 10% 1rst Delivery Lot (+ screening)
  - **PDA (Plan TBC)**
  - **Bonding (tooling, process):** DPD pre-series + mini Xtal
  - **CDE :** DPD pre-series+ Xtal pre-series

Mechanical Structure Manufacturing - LLR

- **Metallic Parts: Aluminum Plates, Titanium Inserts and Nuts**
  - **Contract with the Industry, Includes:**
    - **Fabrication of Parts**
    - **Alodine Surface Treatment of Parts**
    - **100% Verification of Parts**
  - **Proposal Released, Opened to EU Countries – 2 Months for Bids**
  - **Receiving Inspection at LLR, Pre-Assembly (PEM Mechanical and Shipping Configuration), Packaging and Shipping to NRL**
- **Polymer Parts: End Caps, Bumper Frames and Silicone Cords**
  - **Contract with Vendor, ADDIX, Includes:**
    - **Fabrication of Parts**
    - **Verification of Material Properties**
  - **Receiving Inspection at LLR Before Delivery to NRL/CEA**

Mechanical Structure Manufacturing - LLR

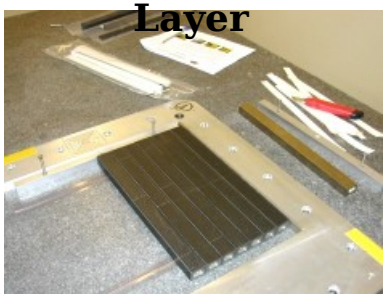
- **Composite Structure**
  - **Procurement of Pre-Preg Material by LLR**
    - **A Procurement of 500 m² is Planned for Flight Structures (20 m² per Structure Required). The Specifications Have Been Released and Accepted by the Vendor, HEXCEL**
  - **Contract for Cutting of Pre-Preg Plies and Preparation of Lay-ups**
    - **The Specifications are Being Updated and Completed, Which Will Require New Proposals**
  - **Structure Fabrication and Verification at LLR**
    - **Two Molds Will Be Used for Flexibility, Which Will Allow a Production Rate of up to One Structure Per Week (If Required)**
    - **Fabrication Will Include the Lay-up of the Pre-Preg Plies in the Molds, the Vacuum Bagging and the Autoclave Curing**
    - **The Verification Will Include:**
      - **Dimensional Inspection**
      - **Measurement of Physical Properties on Co-cured Samples**
      - **Structure Verification Test – Static Pull Test**
  - **Non Destructive Testing**
    - **A Contract for the Ultrasonic C-scan of the Composite Structure (Outer Walls) Is Required. Procedure is Currently Being Evaluated**

Composite Structure – Manufacturing Method

Wrapping of Mandrels

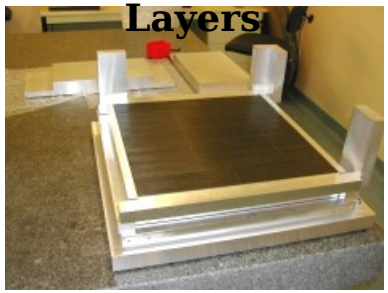
- Each Mandrel Wrapped with One Pre-Preg Ply

Preparation of Layer



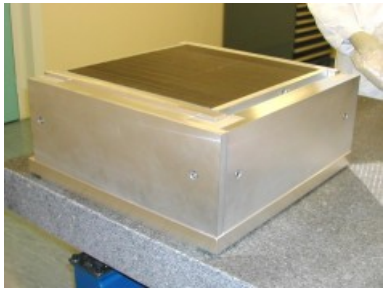
- Stacking of Mandrels and Lateral Lay-Ups with Inserts
- Mechanical Pressure to Add Global Plies

Stacking of Layers



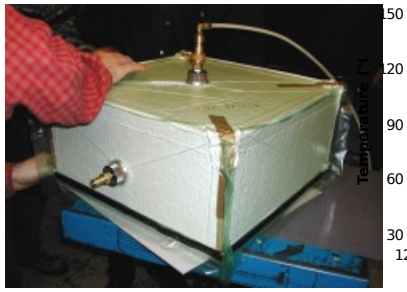
- Stacking of Layers, Base and Top Lay-Ups with Inserts

Closing of Mold



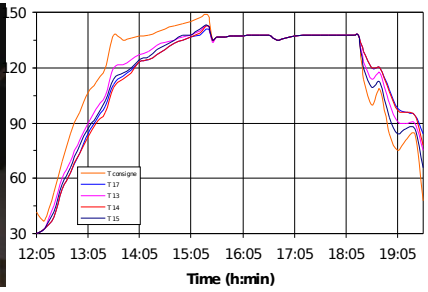
- 4 Side Plates and Cover
- Mechanical Stops to Control Outer Dimensions

Vacuum Bagging



- Release Film
- Breather Felt
- Vacuum Bag

Autoclave Curing

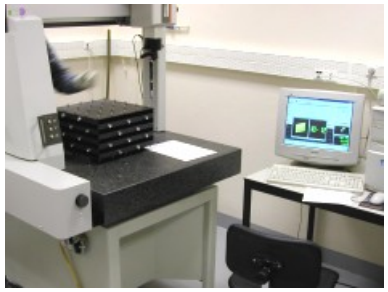


- Temperature 135°C
- Pressure 7 bars
- Cure Time 4h

Structure Removal

- Removal of Layer Frame
- Removal of 96 Mandrels
- Cleaning

Metrology

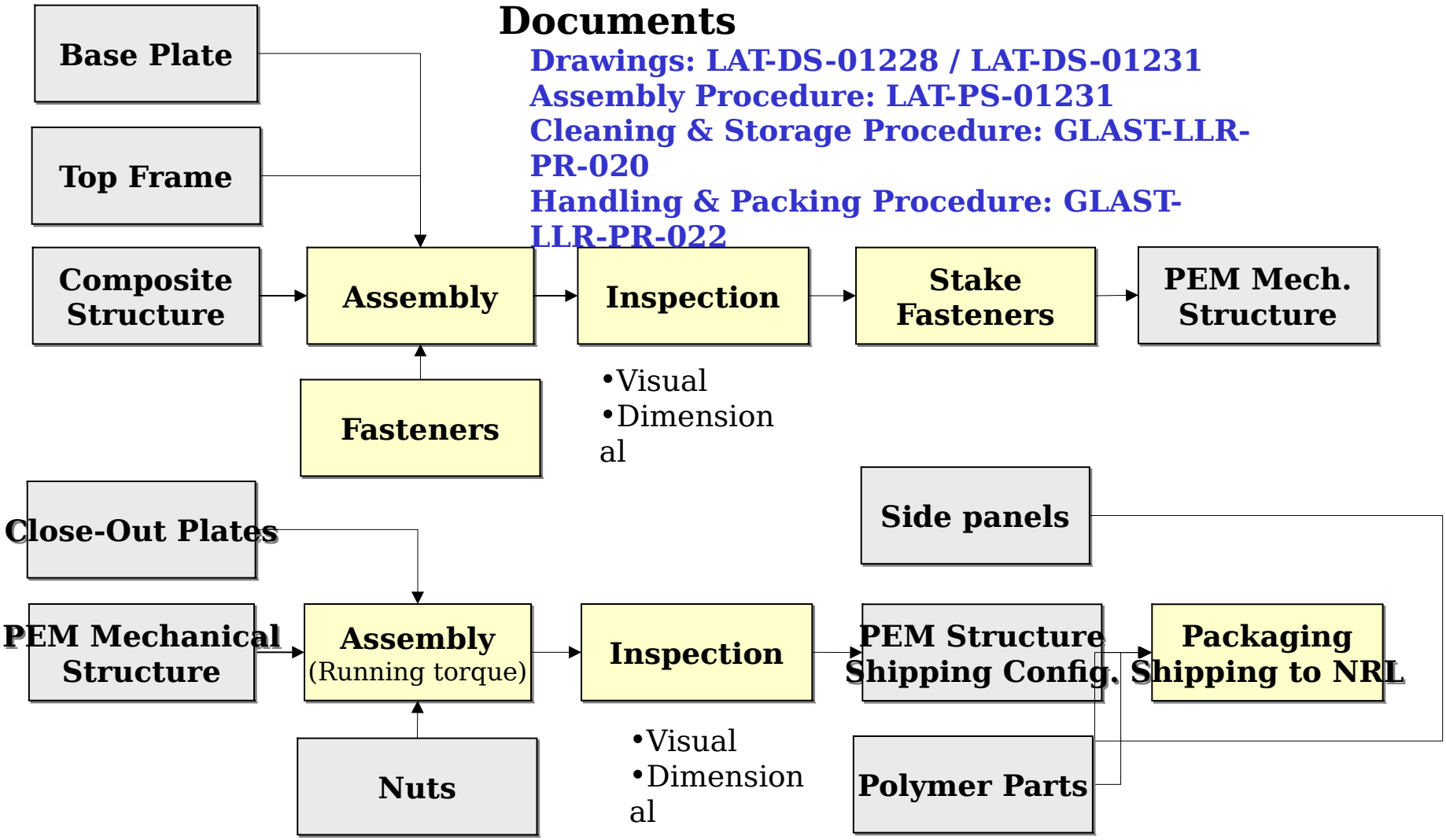


- Outer Dimensions
- Position of Inserts
- Dimension of Cells

Manufacturing
QA Inspection/Verification Testing

COMPONENT	INSPECTION		VERIFICATION TESTING	
	Vendor	IN2P3/LLR	Vendor	IN2P3/LLR
Structural Piece Parts (Aluminum Alloy)	Visual Dimensional (100%)	Visual (100%) Documentation Check	None	None
Titanium Inserts / Nuts	Visual Dimensional (100%)	Visual (100%) Documentation Check	None	Pull Test (sample)
Elastomeric Cords	Visual Dimensional (sample)	Visual (sample) Dimensional (sample) Documentation Check	Tensile Properties Aging (Fabrication Lot)	Tensile Strength Outgassing (Sample/Lot)
End Caps, Bumper Frames	Visual Dimensional (sample)	Visual (100%) Dimensional (sample) Documentation Check	None	None
Composite Structure **- Structure** **- Co-Cured Sample**	N/A N/A N/A	Visual Dimensional (100%) Visual	Ultrasonic C-Scan Material Properties Void Ratio	Static Pull Test

PEM Mechanical Structure Flow

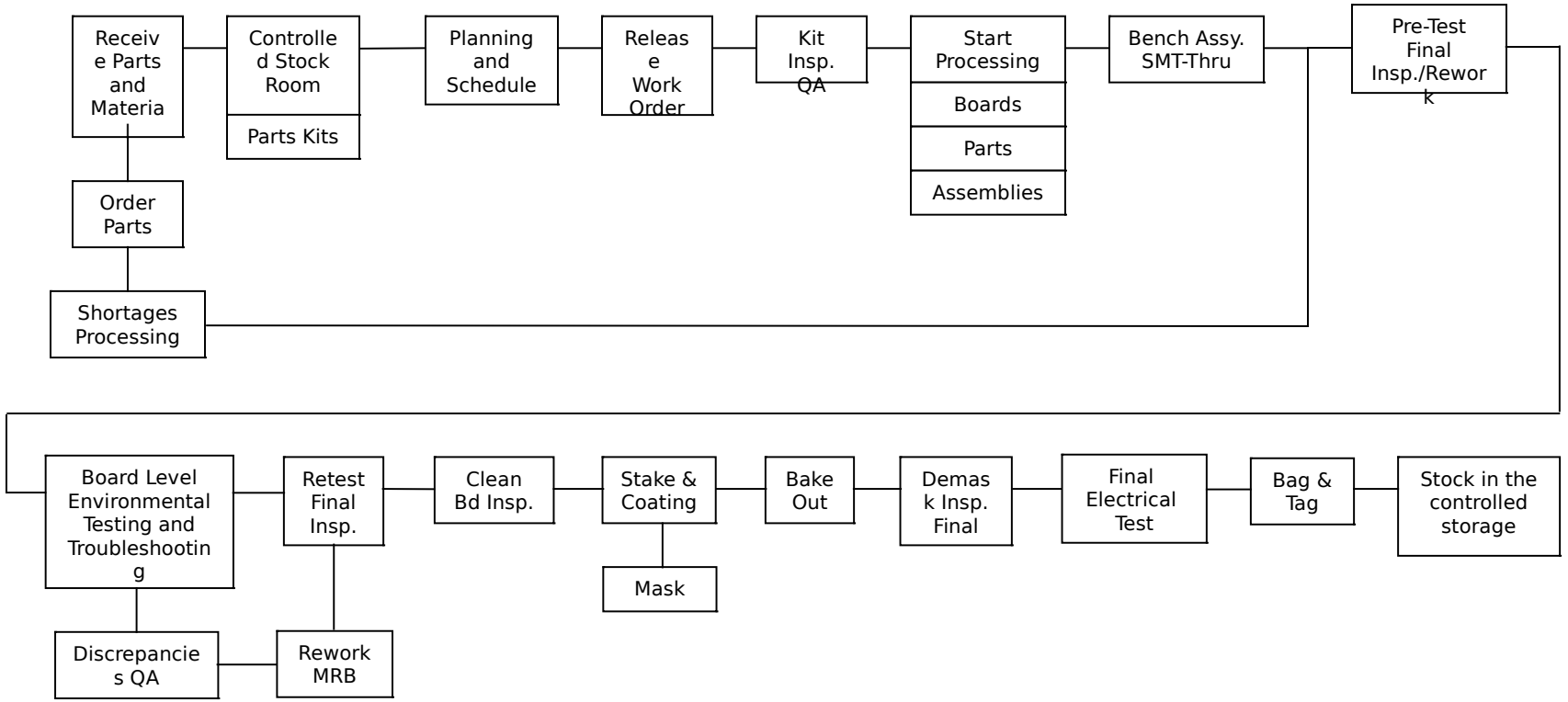


AFEE Board Fabrication

- 100 AFEE Boards to be Assembled by Qualified Vendor
  - All Parts procured & pre-screened by NRL
  - Fabrication process monitored by in-process inspections
- AFEE Boards to undergo rigorous testing
  - Each assembly to be 100% inspected prior to test
  - Boards are thermal-cycled in groups of 12
    - Each board continuously monitored during test
    - Temp extremes of –30 and +85 deg C, w/168 hours accumulated burn-in at 85 deg C
- Testing results analyzed after each group finishes testing
  - Must yield, on average, 9 fully functional boards from each group to maintain Calorimeter Module production schedule
  - Begin rework to those assemblies with the fewest number of parts to replace
    - Use screened, burned-in parts for rework
  - Extent of rework and maximum number of parts allowed to be reworked per assy will be determined by Parts Control Board

AFEE Board Fabrication Process

All work will be performed using approved procedures



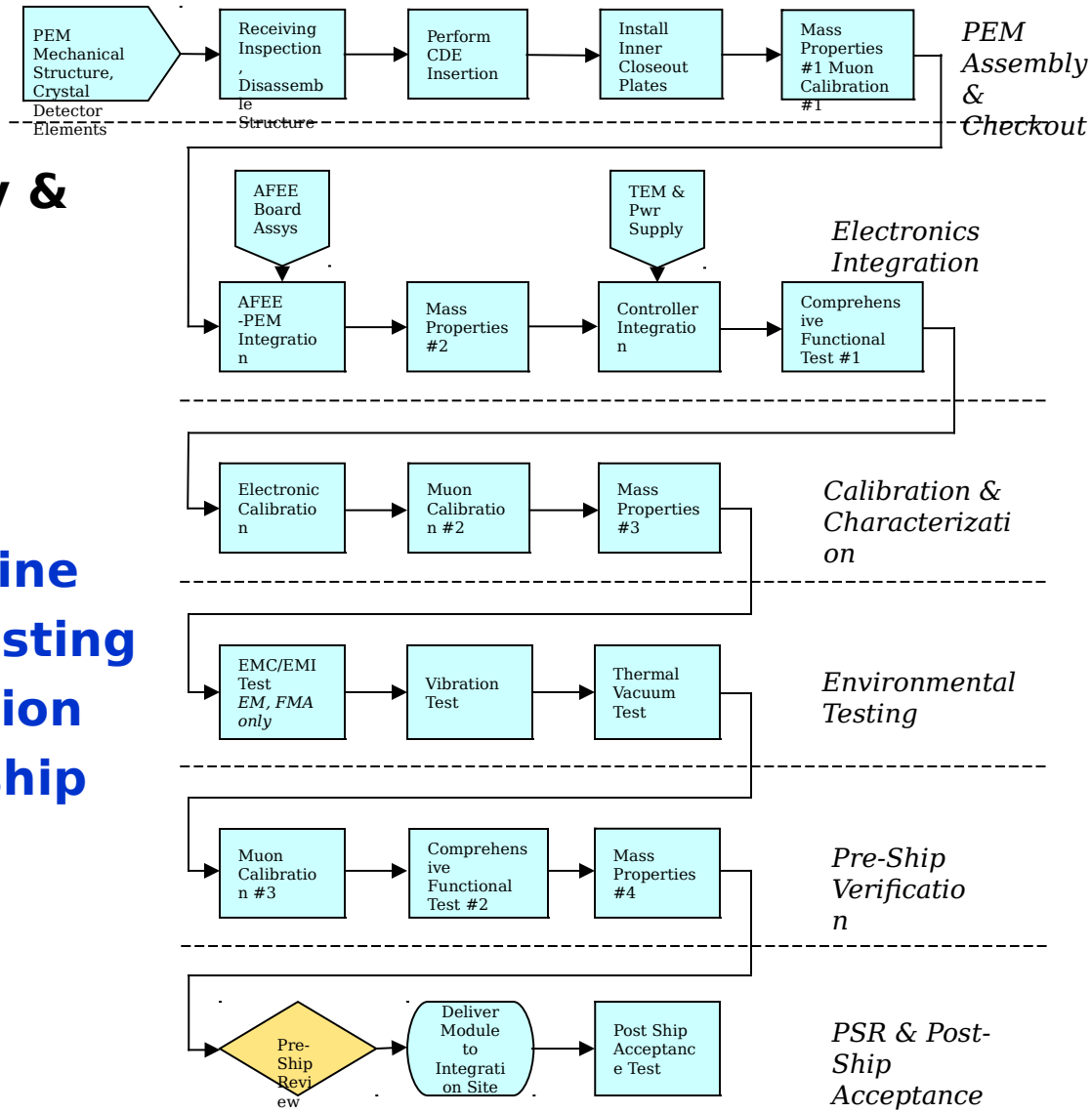
Calorimeter Module Assembly - NRL

- Assemble Calorimeter Tower Modules
  - Pre-Electronics Module
    - Assembled and Tested at NRL
  - Assemble & Test Analog Front End Elect (AFEE) boards
    - AFEE PWB Design, from SLAC
    - ASIC Designs, from SLAC
  - Tower Electronics Module & Power Supply, from SLAC
- Test
  - Functional Testing
  - Environmental Testing
  - Calibration
- Deliver to SLAC
  - Perform Acceptance Test

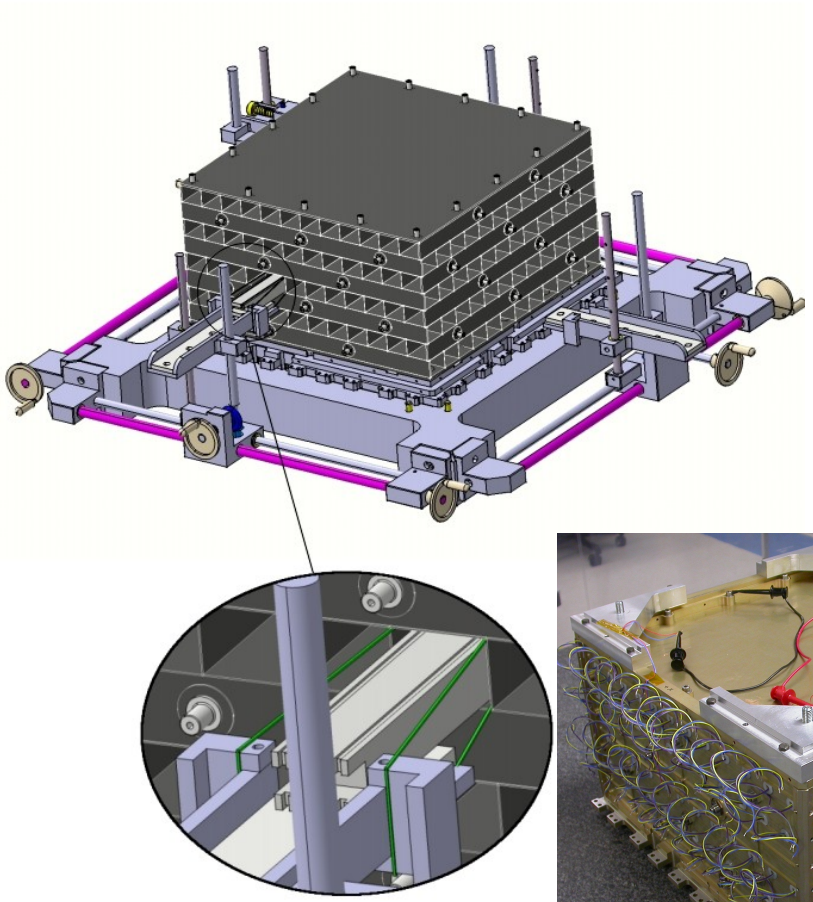
Module Assembly and Test Flow - NRL

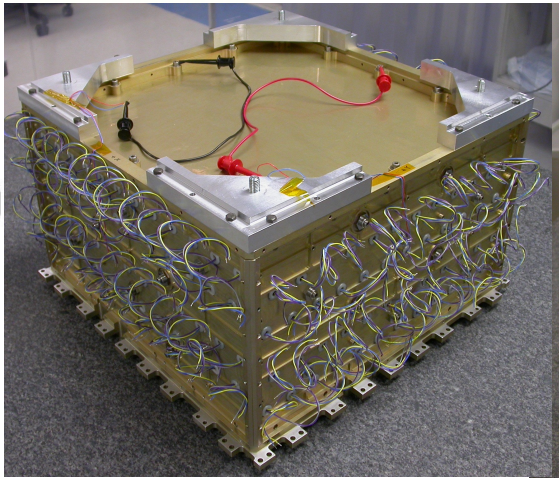
Six Phases in Assembly & Test sequence:

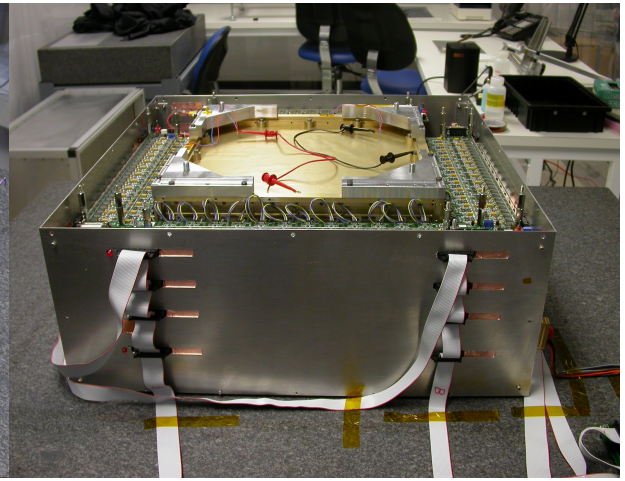
1) **PEM Assembly & Checkout**
2) **Electronics integration**
3) **Calibration/Baseline**
4) **Environmental testing**
5) **Pre-ship verification**
6) **Delivery & Post-ship Acceptance**



PEM Assembly





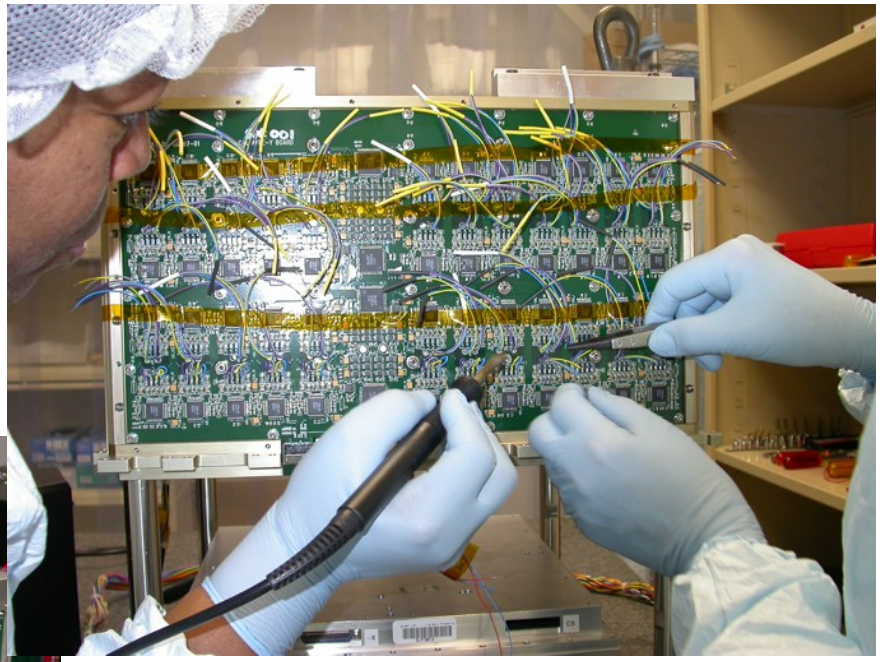


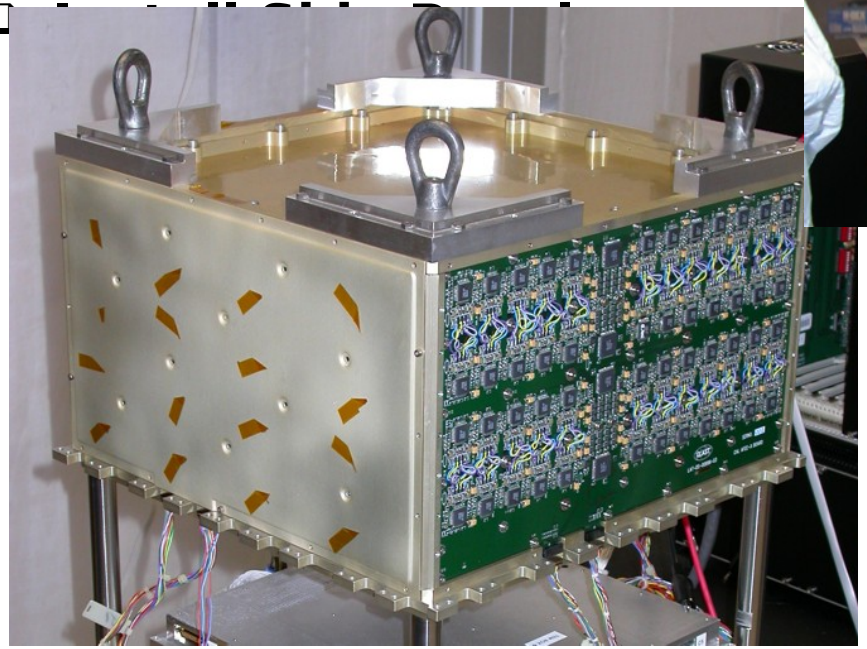
Completed PEM

PEM Acceptance Test

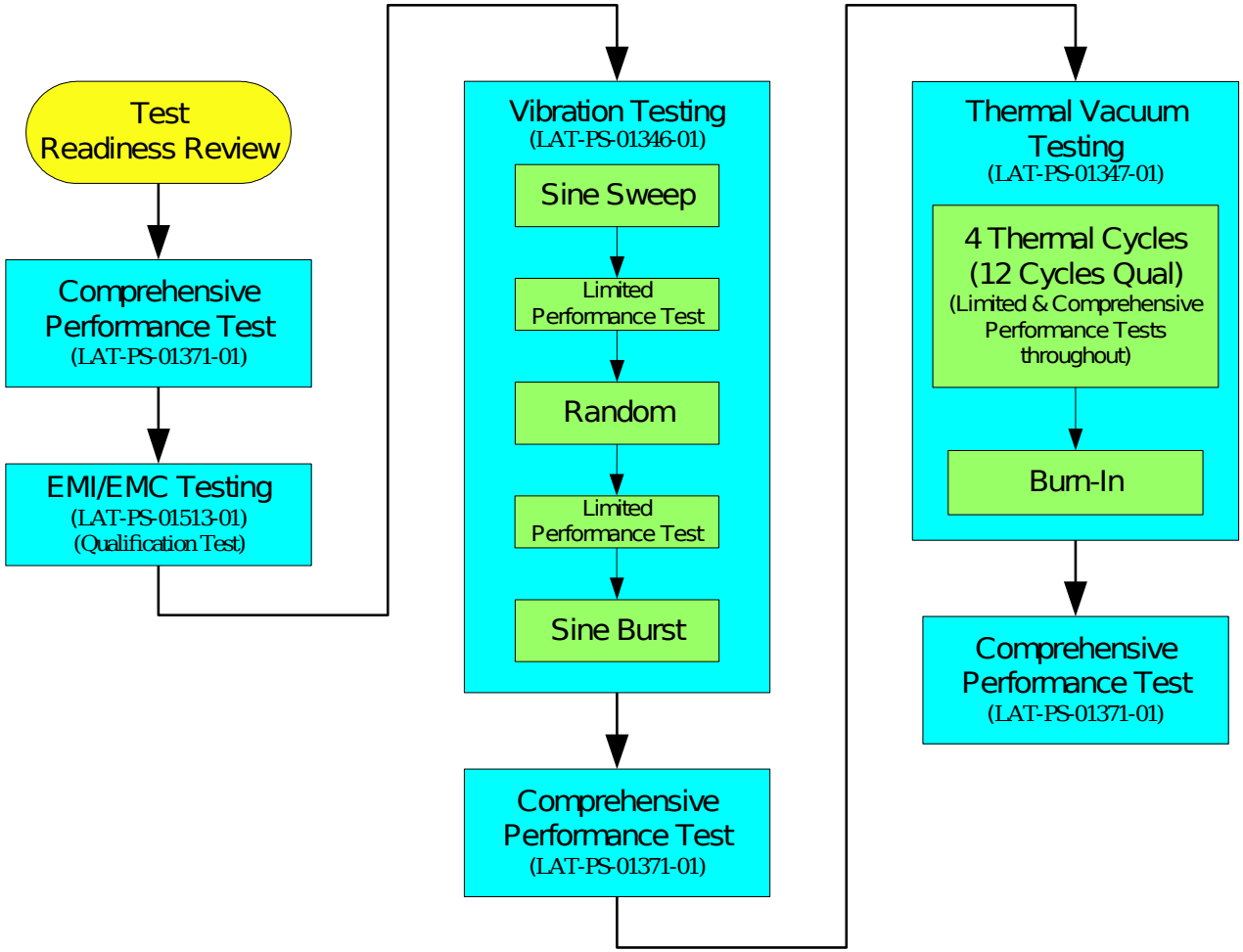
AFEE Board Installation

- Route, dress and solder 192 diode interconnect wires per AFEE board.
- Functional Test
- Stake wires
- [illegible]

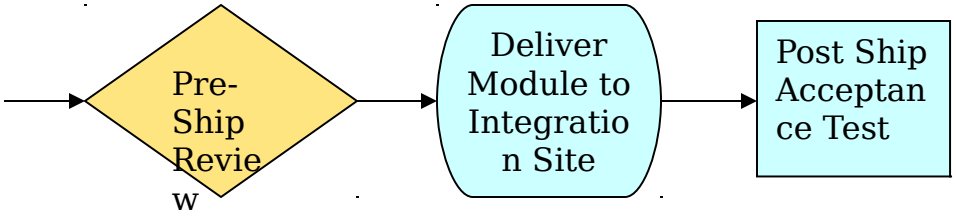




Environmental Test Flow



Delivery & Acceptance



- **Pre-Ship Review**
  - **Review Board consists of Subsystem Manager, A&T Manager, Systems Engineer, QA Engineer, Lead Engineers, others as deemed necessary**
  - **Walk-through A&T flow, review Test Reports, Resolution Reports, status of all anomalies, etc**
- **Flight Unit Delivery**
- **Post-Ship Acceptance Test**
  - **Verifies functionality of delivered CAL Tower Module**
  - **Formal Acceptance by LAT**